RADIATION INTELLIGENT MEMORY CONTROLLER

RIMC VHDL IP CORE
RADIATION HARDENED DDR3 SOLUTION

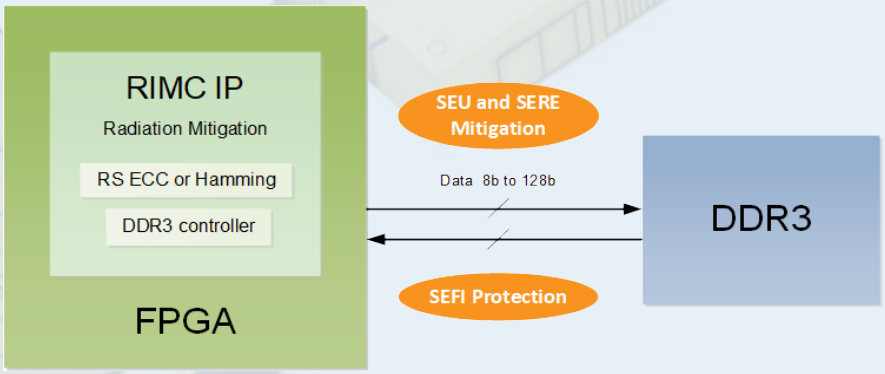
3DIPMC0744-2

PRODUCT OVERVIEW

RIMC DDR3 is a fully configurable DDR3 SDRAM Radiation Intelligent Memory Controller. This IP core is designed to work with 3D PLUS DDR3 memory modules to achieve a global radiation hardened DDR solution.

By its radiation intelligent A.I, this IP Core prevents the DDR3 memory from:

- SEFI: No SEFI were observed up to LET > 60 MeV.cm²/mg.
- SEU/MBU: It mitigates the SEU by using ECCs (Hamming or Reed Solomon) and includes scrubbing mechanisms to correct SEUs and SERE.



KEY FEATURES

- High Performance DDR3 controller w/o ECC
  - DDR Phy interface DFI 2.1 compliant
  - User Interface AMBA compliant AXI/AHB/APB
  - High Speed (up to 800 MHz) DDR3 memory controller
  - Radiation Hardened by Design DDR3 controller
- Radiation Mitigation: already handled – transparent for the user
  - TID Flip bit protection
  - Full SEU protection with ECC: mitigates the SEU by using ECCs (Hamming or Reed Solomon)
  - Scrubbing mechanisms: user definable scrubbing to correct SEUs and SERE.
  - Full SEFI protection, no data loss: no SEFI were observed up to LET > 60 MeV.cm²/mg
- Configurability - Flexibility
  - Variable User data width: from x8bit to x128bit
  - Selectable Hamming or Reed Solomon ECC
  - Selectable burst of 4 or 8 accesses
  - Configurable DRAM refresh time

CORRECTION CAPABILITY VS DATA BUS ORGANIZATION

2 different ECC types are handled by the RIMC:

- Hamming, which is able to mitigate SEU
- Reed Solomon which is able to mitigate SEU, MBU, SERE and SECE

DDR3 COMPONENT WIDTH	DATA BUS WIDTH (DATA_WIDTH)	(ECC_WIDTH)	GLOBAL BUS WIDTH (DQ_WIDTH)	ECC TYPE	CORRECTION CAPABILITY
8	8	0	8	No ECC	None
8	8	8	16	RS(4;2) with m=4	Correct a 4 bits word
8	16	0	16	No ECC	None
8	16	8	24	RS(6;4) with m=4	Correct a 4 bits word
8	16	16	32	2*RS(4;2) with m=4	Correct a 8 bits DDR3 component
8	32	0	0	No ECC	None
8	32	8	40	RS(10;8) with m=4	Correct a 4 bits word
8	32	16	48	2*RS(6;4) with m=4	Correct a 8 bits DDR3 component
8	64	0	64	No ECC	None
8	64	32	96	4*RS(6;4) with m=4	Correct a 16 bits word, (2 contiguous DDR3 components)
8	24/40/48/56 72/80/88/96	0	24/40/48/56 72/80/88/96	No ECC	None
8	128	16	144	2*(Hamming 64+8)	2 bits in error[1]
16	16	0	16	No ECC	None
16	32	0	32	No ECC	None
16	32	32	64	4*RS(4;2) with m=4	Correct a 16 bits DDR3 component
16	64	8	72	Hamming 64+8	Correct 1 bit in error[1]
16	64	32	96	4*RS(6;4) with m=4	Correct a 16 bits DDR3 component
16	48/80/96	0	48/ 80/96	No ECC	None
16	128	16	144	2*(Hamming 64+8)	2 bits in error[1]

[1] This ECC utilizes a Hamming code. This code cannot correct a DDR3 component failure but it is able to correct a SEU.

DDR3 SDRAM MODULES

DDR3 P/N	DENSITY[2] (CONFIGURATION)	VOLTAGE (V)	PACKAGE	TEMPERATURE	SCD#
3D3D16G16YB4751	16 Gbit (1G x 16)	1.35 or 1.5	BGA 95	C, I, S	3DPA-7970
3D3D16G72WB2723	16 Gbit (256M x 72)	1.35 or 1.5	BGA 199	C, I, S	3DPA-7410
3D3D24G48YB2732	24 Gbit (512M x 48)	1.35 or 1.5	BGA 259	C, I, S	3DPA-8141

[2] Max Data for user

TEMPERATURE RANGES
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
S: Specific (-40°C to +105°C)

RADIATION HARDENED DDR3 SOLUTION

PARAMETER	CONDITIONS	VALUE	UNIT
TID	-	> 75	krad(Si)
SEL	-	> 67	MeV.cm²/mg
SEU/SERE/SECE	Immune with 3DIPMC0744 embedded RS ECC		
SEFI	Immune with 3DIPMC0744 protection	> 60	MeV.cm²/mg

FPGA target availabilities:

- Xilinx: Series 7, Ultrascale
- Microchip: RT Polarfire under development

ORDERING INFORMATION
Part Number: 3DIPMC0744 – X
Revision

3D plus a HEICO company

www.3d-plus.com