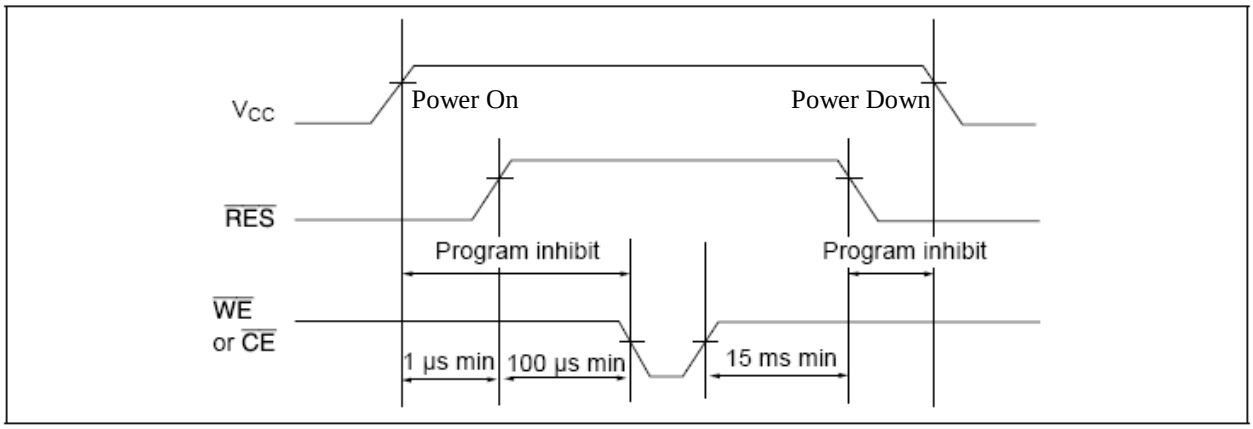
EEPROM Modules
Data Protection at Vcc On/Off

Revision history:
Rev 1: Document initial
Rev 2: Precise Power On sequence

3D Plus EEPROM Modules have been used to save critical data for space missions with years' flight heritage. This document describes how to use RES pin to prevent unintentional programming to protect the critical data saved in the EEPROM Modules.

As the well know reason of the charge pump inside of the EEPROM, when Vcc is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM modules to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state. The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's RES pin: During Power On, RES should be asserted at Vss level (less than or equal to 0.5V) untill at least 1 micro second after Vcc rises above Vccmin(2.7V). During Power down, RES should be at Vss level before Vcc falls below Vccmin(2.7V), and hold Reset asserted during Power down until Vcc falls to less than 1V.



To high reliability space mission's critical data protection, RES can be asserted at Vss level except EEPROM Read/Write operations to maximum the EEPROM module data protection.