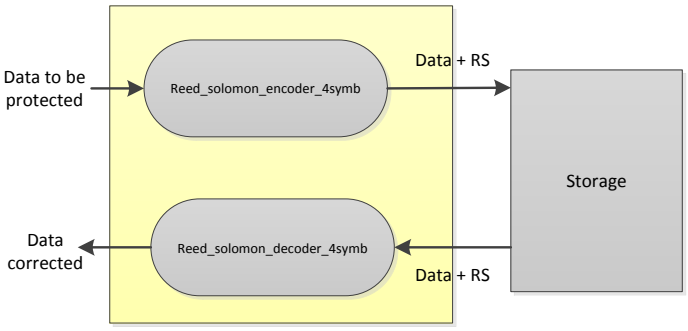
**Reed Solomon 4 symbols**

# 3DIPEC0726-1

**2 symbols correction capacity Reed Solomon**

## FEATURES

- Configurable input data size
- Configurable ECC size
- 2 symbol correction capacity, symbol size is a quarter of the ECC size
- Decoder indicates when a symbol is corrected
- Decoder indicates when an incorrigible error is detected
- Encoder is a combinatory entity
- Configurable output delay for decoder




## GENERAL DESCRIPTION

3DIPEC0726-1 is a Reed Solomon encoding and decoding IP core designed to provide protection for data storage in space applications.

Reed Solomon is a block code, the transmitted codeword is divided in block of data called symbols. Symbols are coded on several bits as elements of a Galois field. The Reed Solomon IP is based on the Galois field GL(2^4), symbols are coded on 4 bits and the maximum size of a message after encoding is 15 symbols (60 bits).

The Reed Solomon IP core offers the possibility to address data bus with more than 60 bits by implementing several encoder or decoder inside the same IP. Thus the size of a symbol is a quarter of the ECC size.

To be able to detect and correct 2 symbols in error, 4 symbols are added to the codeword.

The Reed Solomon decoder indicates when an incorrigible error is detected. An incorrigible error is when at least two symbols have been modified. Not all of incorrigible errors are detected.

The Reed Solomon decoder has a configurable output delay in number of clock cycle. Add delay enables the decoder to reach higher clock frequencies.

The IP provide two entities, the encoding entity *reed_solomon_encoder_4symb* and the decoding entity *reed_solomon_decoder_4symb.*

# PINOUT AND GENERICS DESCRIPTION

| Ports or Generics | Direction | Comments |
|---|---|---|
| DATA_WIDTH | generic | Data bus size in bits<br>The DATA_WIDTH value must be a multiple of 4 between 16 and 44 if ECC_WIDTH =16<br>The DATA_WIDTH value is a multiple of 8 between 32 and 88 if ECC_WIDTH =32 |
| ECC_WIDTH | generic | ECC bus size in bits<br>The ECC_WIDTH generic value can be 16 or 32. |
| Data_input | in | Data to be encoded |
| Data_output | out | Data encoded |

Table 1: pinout and generic of reed_solomon_encoder_4symb

| Ports or Generics | Direction | Comments |
|---|---|---|
| DATA_WIDTH | generic | Data bus size in bits<br>The DATA_WIDTH value must be a multiple of 4 between 16 and 44 if ECC_WIDTH =16<br>The DATA_WIDTH value is a multiple of 8 between 32 and 88 if ECC_WIDTH =32 |
| ECC_WIDTH | generic | ECC bus size in bits<br>The ECC_WIDTH generic value can be 16 or 32. |
| CLK_DELAY | Generic | Number of clock cycle delay between input and output<br>The CLK_DELAY generic is between 0 and 3 |
| GSYNCRST | Generic | Synchrone or asynchrone reset |
| SysClk | in | System clock |
| Rst_N | in | Input reset active LOW |
| Data_input | in | Data to be decoded |
| Data_output | out | Data decoded |
| errorc | out | Is set when a corrigible error is detected |
| errornc | out | Is set when an uncorrigible error is detected |

Table 2: pinout and generic of reed_solomon_decoder_4symb

## RESOURCES AND TIMING

Following results have been perfom on both encoder and decoder with DATA_WIDTH =44 and ECC_WIDTH = 16 and CLK_DELAY = 0 for the decoder.

The size and delay depend on generics configuration.

| FPGA | Number of LUTs | Propagation delay |
|---|---|---|
| Virtex5 | 1157 | 17.7ns |
| RTG4 | 1596 | 34ns |

Table 3: ressource used and propagation delay for reed_solomon_decoder_4symb

| FPGA | Number of LUTs | Propagation delay |
|---|---|---|
| Virtex5 | 82 | 2.3ns |
| RTG4 | 105 | 4.4ns |

Table 4: ressource used and propagation delay for reed_solomon_encoder_4symb

### ORDERING INFORMATION

| Part number | 3DIPEC0726-1 |
|---|---|

**Main Sales Office:**

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