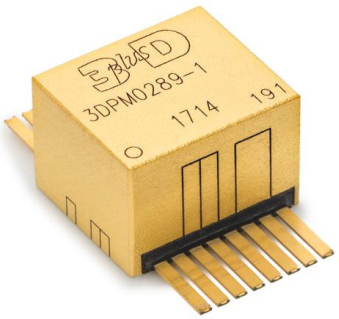
HI-REL PoL DC/DC CONVERTER

4.5V to 12V Input, 1V to 5V Single Output

3DPM0289-1



1. GENERAL DESCRIPTION

The 3DPM0289-1 PoL DC/DC Converter, operates over a wide input voltage range (4.5 V to 12 V) and provides up to 1.9 A of output current with an output voltage range of 1 V to 5 V.

Based on a Buck topology, the PoL module uses synchronous rectification to boost efficiency higher than 90% (3.3 V/0.3 A to 1.5 A). Switching frequency is fixed at 340 kHz. EMC filters are integrated to simplify module implementation and output voltage is adjustable through an external resistor. Module is fully protected against output overload, input under-voltage and internal over-temperature.

Featuring specific radiation effect mitigation techniques and utilizing space design de-rating rules, the PoL Converter features a SEL LET threshold of 60 Mev.cm2/mg and a TID of 40 krad (Si).

The 3DPM0289 module is based on 3D PLUS's stacking technology - which is qualified for harsh environments (able to withstand appreciable mechanical shock and vibration) - and also leverages 3D PLUS's extensive experience in Space product design and component selection, yielding a highly reliable, Space qualified PoL with unprecedented power density and efficiency.

2. KEY FEATURES

- Input voltage range: 4.5 V to 12 V
- Adjustable output voltage: 1 V to 5 V
- Output current up to 1.9 A
- Efficiency > 90% (3.3 V, 0.3 A to 1.5 A)
- Integrated I/O filters
- Configurable protections:
  - Input UVD
  - Output over-current and over-voltage
  - Internal over-temperature
- Parallelization capability
- Soft-start, Enable command
- Fixed switching frequency (340 khz)
- Excellent Dynamic Performances
- Radiation Hardened by Design:
  - TID > 40 krad(Si)
  - SEL LET > 60 MeV.cm^2.mg^{-1}
  - SET Immune
- Operating temperature -40 °C / +85 °C
- 16-Gull-Wing package
- Size: 12.5 x 11 x 9.4 mm
- Mass: < 4 g

3. APPLICATIONS

- Low voltage power supply for FPGA, ASICs and memory banks
- Distributed Power Architectures for Space applications

TABLE OF CONTENTS

TABLES AND FIGURES

4. TYPICAL APPLICATION SCHEMATIC

4.1 RECOMMENDED SCHEMATIC

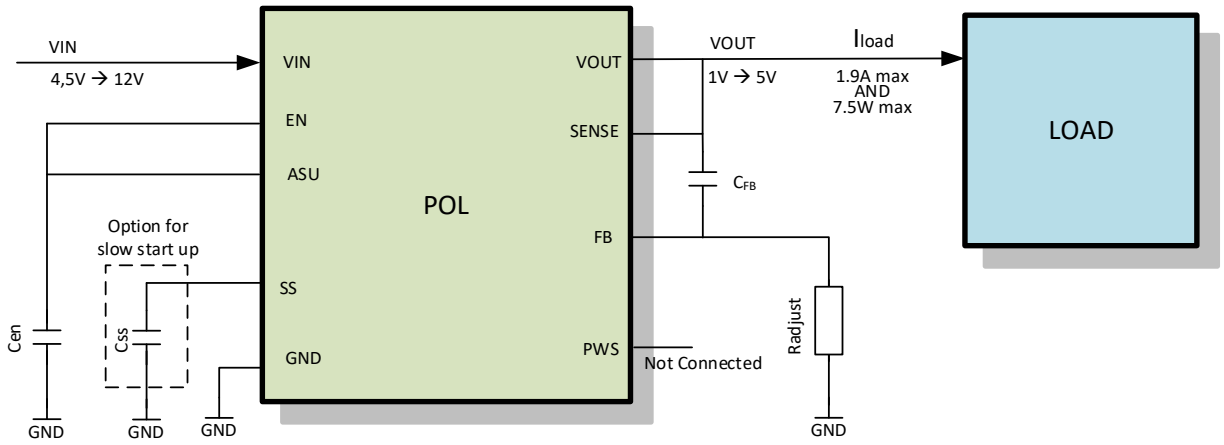


Figure 1 : Typical application schematic of the 3DPM0289-1

C_{en} = 100 nF and C_{FB} = 22 nF

4.2 PARALLEL CONFIGURATION

For increased output current, two PoL modules can operate in parallel configuration to achieve up to 3.8 A. No external component needs to be added. Only PWS pins must be connected together, making possible an equitable sharing of the current between the two PoL converters. The circuit configuration for paralleling PoL is the following one:

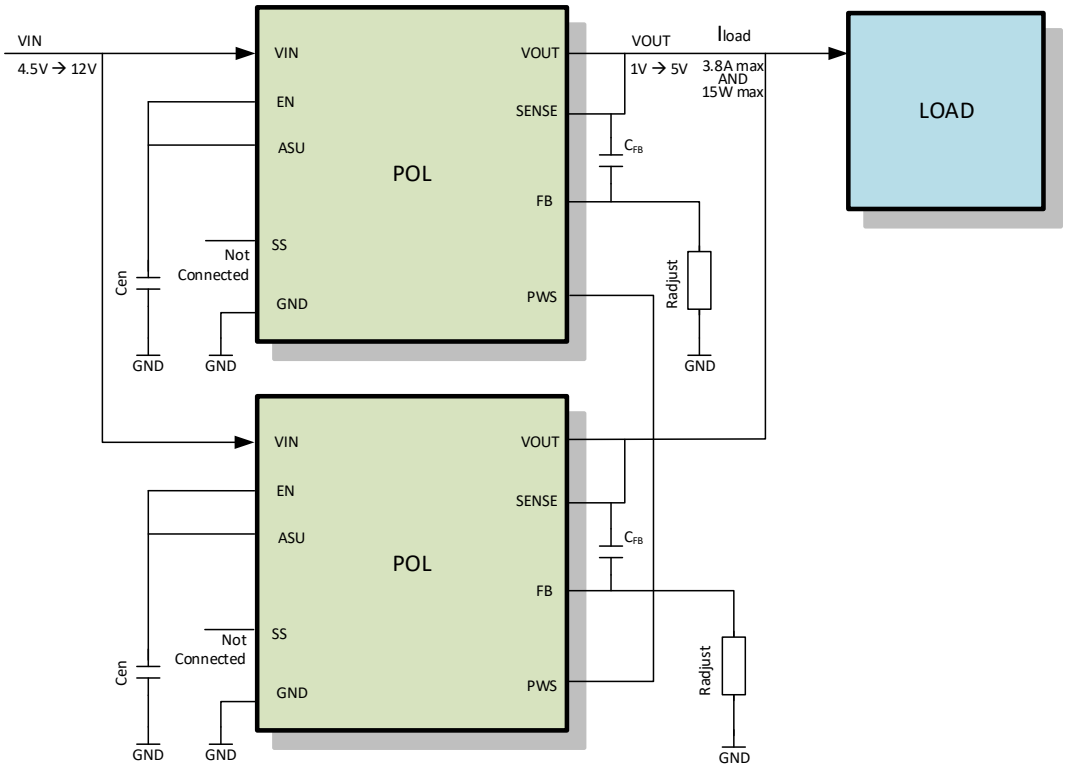


Figure 2 : Typical application schematic of two 3DP0289-1 in parallel configuration

Each FeedBack pin shall be connected to GND through a resistor (the two resistors must have the same value) placed as close as possible to the module.

5. PINS DEFINITION and ASSIGNMENTS

SYMBOL	TYPE	NUMBER	FUNCTION
GND	Input	1; 8; 9; 10; 11	Reference ground for the PoL module. Shall be connected on large PCB ground plane for optimal heat dissipation.
PWS	Input	2	Power sharing pin for module parallelization. Connect PWS pins of each module to ensure parallel operation of the PoLs. Left open otherwise.
ASU	Input	4	Automatic Start-Up pin. This pin may be connected to the EN pin to set an automatic start-up. An internal 100 kΩ pull-up resistor is connected to VIN. In this case is recommended to add a capacitance of 100 nF between ground and ASU to delay start-up.
FB	Input	12	FeedBack pin. FB pin senses the output voltage in order to regulate the voltage. The An external 22 nF capacitor shall be connected between FB and SENSE pins. FB pin shall be connected to GND thru a resistor.
SS	Input	3	Soft-start control pin. The SS pin controls the soft-start period. An internal 47 nF capacitor sets the soft-start period to 4 ms by default. A capacitor may be connected from the SS pin to the GND pin to increase the soft-start period.
SENSE	Input	13	Sense pin. Used to sense the output voltage for improved accuracy. It can be connected to VOUT pins for local sensing or connected to VOUT at load location for remote sensing.
VIN	Input	6; 7	Power input voltage pins. DC supply for the PoL module.
EN	Input	5	Enable command. EN pin is a digital input pin that enables or disables the regulator. For an automatic start-up the ASU pin must be used.
VOUT	Output	14; 15; 16	Power output voltage pins. This voltage can be adjusted through the FB pin from 1 V to 5 V.

Table 1: Pins description

6. SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Operation beyond the following limits may cause module degradation, affect module reliability or cause permanent damage to the module.

Parameter	Symbol	Conditions	Min	Max	Unit
Input Voltage	V_{IN}	Continuous	-0.3	15	V
Enable Voltage	V_{EN}	Continuous	-0.3	5.5	V
Output Current	I_{OUT}		0	2.7	A
Output Power	P_D			7.5	W
Storage Temperature	T_{STG}		-55	+150	°C
Junction Temperature	T_J		-40	+125	°C

Table 2: Absolute maximum ratings

6.2 RECOMMENDED OPERATING CONDITIONS

For proper operation, the module should be used within the recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
Input Voltage (Note 1)	V_{IN}	4.5	12	V
Enable Voltage	EN (OFF state)	0	1.1	V
	EN (ON state)	2.7	5.5	V
Output Voltage (Note 1)	V_{OUT}	1	5	V
Output Current (Note 1)	I_{OUT}	0	1.9	A
Thermal Resistance Junction to Case	$R_{TH(J-C)}$		20	°C/W
Thermal Resistance Junction to Ambient	$R_{TH(J-A)}$		25	°C/W
Operating Temperature	T_{OP}	-40	105	°C

Table 3: Recommended operating conditions

Note 1: The range of use is specified in Figure 3 and Figure 4 (Input Voltage, Output Voltage and Output Current).

6.3 MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Parameter	Conditions	Min	Typ	Max	Unit
Weight				4	G
Parameter	**Conditions**	**Typ**			**Unit**
Dimensions	Body	12.5 (L)	11 (W)	8.9 (H)	mm

Table 4: Mechanical specifications

Parameter	Conditions	Min	Typ	Max	Unit
Total Irradiation Dose		40			krad(Si)
SEL LET Threshold		60			MeV.cm²/mg
SET LET Threshold		60			MeV.cm²/mg

Table 5: Environmental specifications

The PoL Converter module includes several active components in addition to the ASIC that have been tested under irradiation (TID, SEL and SET).

6.4 INPUT & OUTPUT SPECIFICATIONS

Parameters are defined over the specified input voltage, output load and temperature range unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Voltage Range	V_{IN}		4.5		12	V
Input Current	I_{IN}	V_{IN} = 5 V, V_{OUT} = 3.3 V, no load, EN = 3.0 V (enabled)			8	mA
Standby Current	$I_{STANDBY}$	V_{IN} = 5 V, V_{OUT} = 3.3V, no load, EN = 0 V (disabled)			30	µA
Output Characteristics						
Output Voltage	V_{OUT}		1		5	V
Output Voltage Accuracy (Note 2)		V_{IN} = 5 V, V_{OUT} ≤ 1.2 V,	-2.0		2.0	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		I_{OUT} = 500 mA				
		V_{IN} = 5 V, V_{OUT} > 1.2 V, I_{OUT} = 500 mA	-2.15		2.15	%
Output Current	I_{OUT}		0.0		1.9	A
Load Transient		I_{OUT} =±1 A, di/dt = 10 A/µs (min DC load = 500 mA)		75	100	mV
Line Regulation		V_{IN} = 4.5 V to 12 V			-0.2	%/V
Load Regulation		I_{OUT} = 0 to 500 mA			-3	%/A
		I_{OUT} = 500 mA to 1.9 A			-1.25	%/A
Output Ripple		Measurement BW limited to 20 MHz I_{OUT} = 1.5 A			12	mVrms
					80	mVpp
		Measurement BW limited to 20 MHz I_{OUT} = 1.9 A			12	mVrms
					80	mVpp
Switching Frequency	F_{SW}			340		kHz
Efficiency	η	V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA	90	94		%
		V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1.9 A	82	87		%
		V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 1.5 A	84	89		%

Table 6: Input and output specifications

Note 2: This value does not take into account external resistor accuracy.

6.5 COMMANDS AND PROTECTIONS SPECIFICATIONS

Parameters are defined over the specified input voltage, output load and temperature range unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overload Protection						
Maximum Output Current	I_{MAX}	Output voltages starts dropping	1.9			A
Undervoltage Protection						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
UVD Protection Threshold		V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A	3.5		4.1	V
UVD Recovery Threshold		V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A	3.8		4.48	V
UVD Hysteresis				220		mV
Internal Temperature Protection						
Internal Thermal Shutdown Temperature				160		°C

Table 7: Commands and protections specifications

6.6 RANGE OF USE

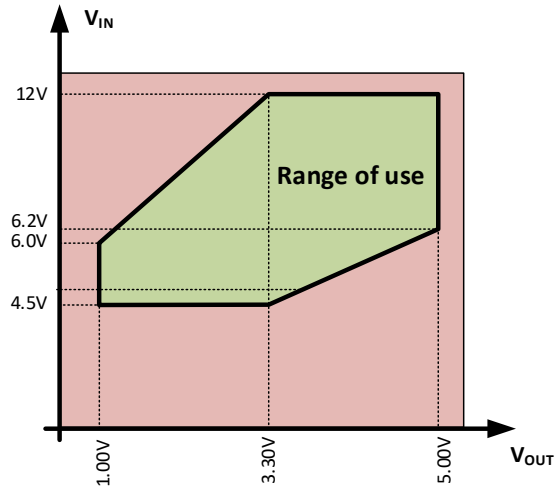


Figure 3: Input voltage vs. output voltage

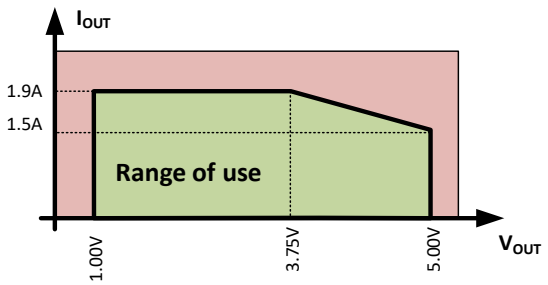


Figure 4: Output power vs. output voltage

7. BLOCK DIAGRAM

The block diagram of the PoL is shown hereafter:

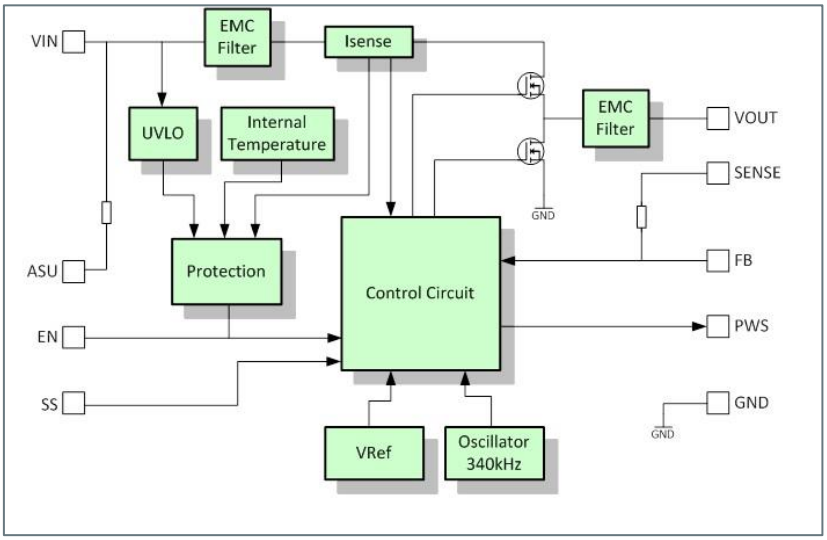


Figure 5: Functional block diagram

8. FEATURES DESCRIPTION

Output Voltage Setting:

The output voltage is adjusted by setting a resistor value between the FB pin and ground. Resistor value is selected according to the following formulae, to reach the output voltage accuracy performances:

$$V_{out} = 0.920 * \frac{(R_{adj} + 5920)}{R_{adj}} \quad (1)$$

$$R_{adj} = \frac{5920 * 0.920}{V_{out} - 0.920} \quad (2)$$

Example:

- for V_{OUT} = 1.0 V, use R_{ADJ} = 68.1 kΩ
- for V_{OUT} = 1.8 V, use R_{ADJ} = 6.19 kΩ
- for V_{OUT} = 2.5 V, use R_{ADJ} = 3.48 kΩ
- for V_{OUT} = 3.3 V, use R_{ADJ} = 2.26 kΩ

All resistors mentioned above are selected from E48 series.

Output Voltage Accuracy:

Output voltage accuracy can be determined by adding 3DPM0289-1 contribution (as specified in output specifications section) to R_{ADJ} contribution.

Example:

A 2.26 kΩ adjustment resistor (R_{ADJ}) is used. Its end-of-life accuracy is (+1.0 %/-2.0 %).

Typical output voltage in this configuration is:

$$V_{out-typ} = 0.920 * \frac{(2260 + 5920)}{2260} = 3.330\ V$$

3DPM0289 contribution to output voltage accuracy is ± 2.15 %:

$$\Delta V_{out}(3DPM0289) = \pm\ 2.15\ \% * 3.329 = \pm\ 72\ mV$$

R_{ADJ} resistor contribution is:

$$\Delta V_{out-p}(R_{adj}) = V_{out}(R_{adj-min}) - V_{out-typ} = 0.920 * \frac{(2260 * 0.98 + 5920)}{2260 * 0.98} - 3.330 = +49\ mV$$

$$\Delta V_{out-n}(R_{adj}) = V_{out}(R_{adj-max}) - V_{out-typ} = 0.920 * \frac{(2260 * 1.01 + 5920)}{2260 * 1.01} - 3.330 = -24\ mV$$

Overall output voltage accuracy is the sum of the two contributions:

$$\Delta V_{out-p} = 72 + 49 = +121\ mV$$

$$\Delta V_{out-n} = 72 + 24 = -96\ mV$$

9. PROTECTIONS

Output Overload Protection:

An internal current protection at 2 A threshold is included. This protection is a current control mode and in case of overload, the duty cycle of the converter is limited and the output voltage decreases.

Input Undervoltage Protection:

An input under voltage lockout is provided and the module is switched off in case the input voltage decreases under 4.1 V.

Internal Temperature Protection:

A thermal sensor is included inside the module, close to the switching transistors in order to provide an internal thermal protection. The protection is triggered when temperature reaches 160 °C ± 15 °C.

EMC Filters:

The PoL converter includes input and output filters to withstand the input/output inrush currents and to avoid differential mode susceptibility. The switching frequency of the Buck regulator is fixed at 340 kHz and the output filter guaranteed an output noise of 20 mV at maximum frequency.

EMC filters are integrated into the module preventing the use of external filters, saving PCB area and making converter design and integration much easier.

10. TYPICAL ELECTRICAL PERFORMANCES

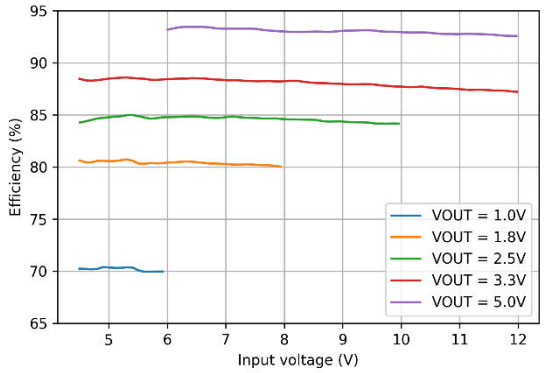


Figure 6: Efficiency @ I_{OUT} = 1.9A / V_{OUT} = 1 V, 1.8 V, 2.5 V, 3.3 V and 5 V, V_{IN} = 4.5 V to 12 V.

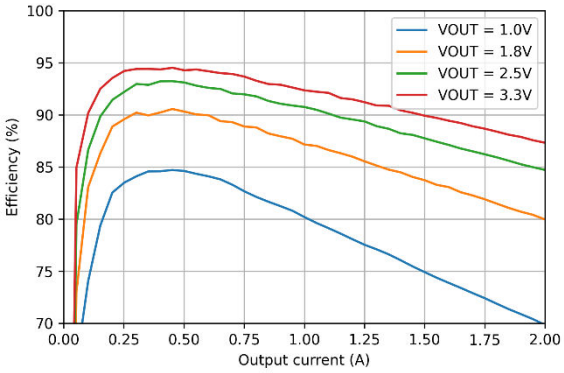


Figure 7: Efficiency @ V_{OUT} = 1 V, 1.8 V, 3.3 V and 2.5 V / I_{OUT} up to 2 A / V_{IN} = 5.0 V

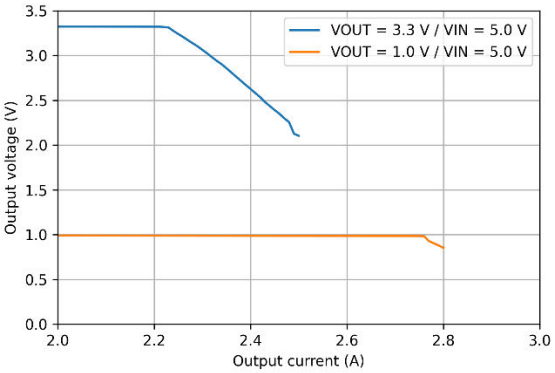


Figure 8 : Output voltage profile in current limitation @ V_{OUT} = 1 V, 3.3 V / V_{IN} = 5.0 V

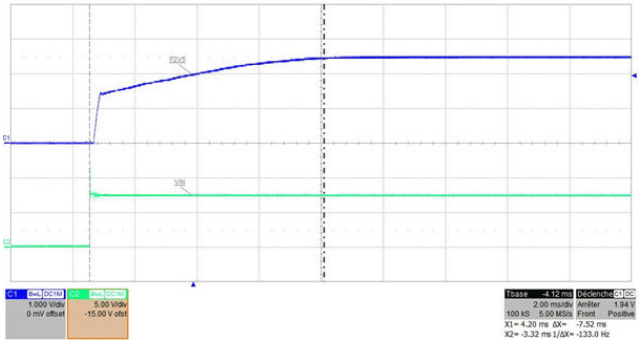


Figure 9 : Start-up trough ASU
C1 = V_{OUT} (1 V/div); C2 = V_{IN} (5 V/div); X= 2 ms/div

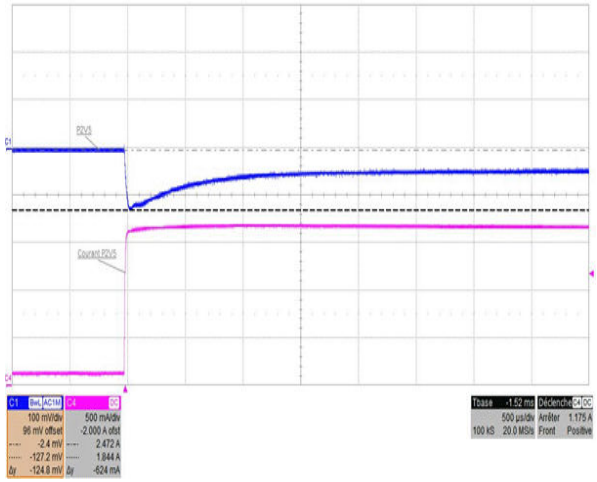


Figure 10 : Load Regulation for I_{OUT}: 100 mA to 2 A
C1 = V_{OUT} (100 mV/div); C2 = I_{OUT} (500 mA/div)

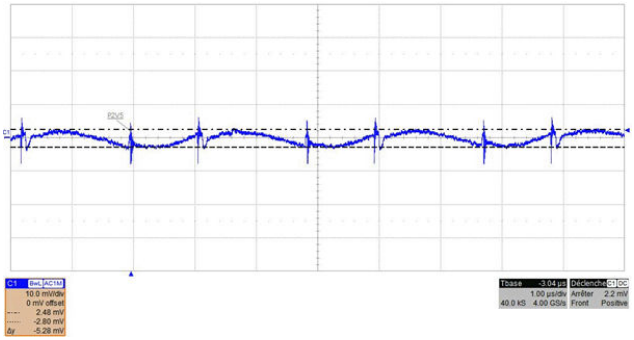


Figure 11 : Switch Output Noise for V_{IN} = 7.5 V, V_{OUT} = 2.5 V
I_{OUT} = 1.9 A @ 340 kHz
C1 = V_{OUT} (10 mV/div)

11. LAYOUT RECOMMENDATIONS

The module is a non-isolated synchronous buck converter. It shall be mounted over a common ground plane and connected to the case of the module. Moreover, all GND pins shall be connected together to the dedicated ground plan.

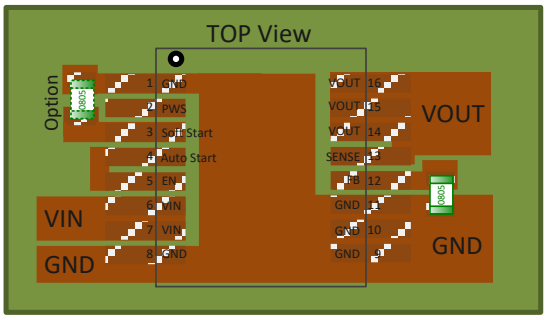


Figure 12 : Recommended Layout for PoL module

The resistor connected to the FeedBack pin, shall be connected as close as possible to the module in order to avoid the noise that could be generated from the regulation loop. The FeedBack pin is directly connected to the input of the error amplifier and this pin is very sensitive. Large tracks shall be used for Vin and Vout pins.

In case of two PoL working in parallel, the connection between each PoL shall be as short as possible, as show in the following layout.

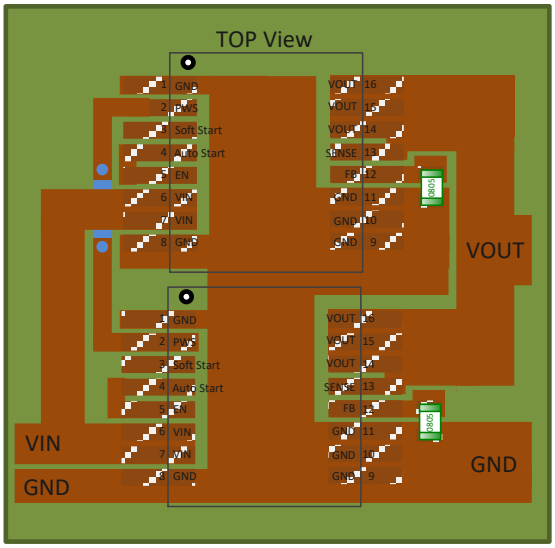


Figure 13 : Recommended Layout for two PoL modules

12. MODULE MECHANICAL DRAWING (mm)

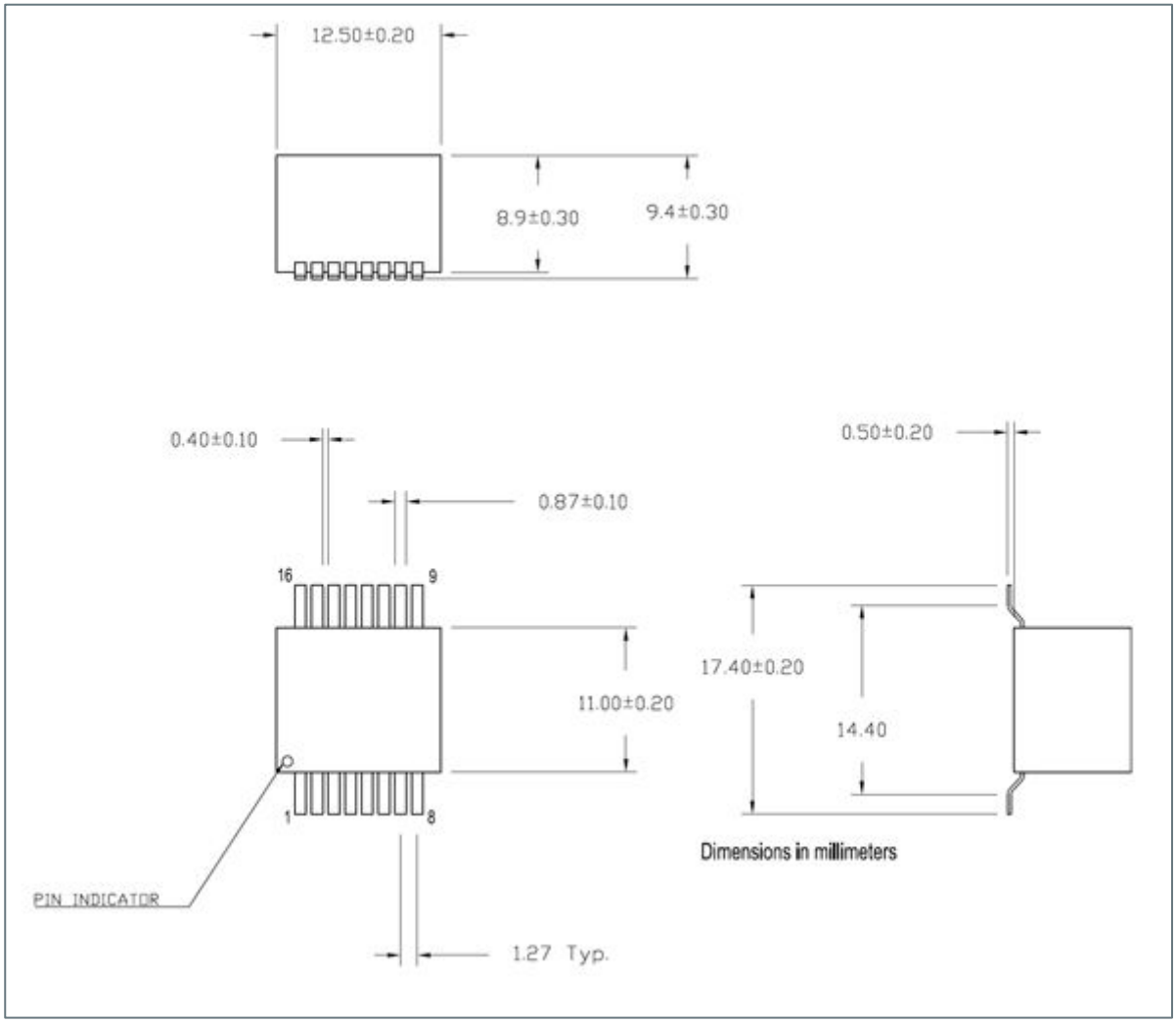
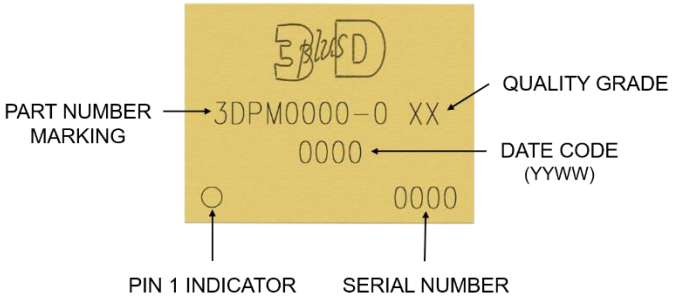


Figure 14: Mechanical drawing

Note: Module assembly must follow reflow guidelines as defined in 3300-1300 document:

https://www.3d-plus.com/customer-service/#assembly_recommendation

13. PART NUMBER / ORDERING INFORMATION



3DPM0289-1 X X

Temperature range

C = (0°C to +70°C)
I = (-40°C to +85°C)

Screening level

N = Commercial grade
B = Industrial grade
S = Space Grade

14. REVISION HISTORY

Ed./Rev.	Date (Dd/Mm/Yyyy)	Description
11	10/01/2025	This document replaces 3DFP-0680-10. I_{OUT} max limit change from 2 A down to 1.9 A in all document. Schematics updated with C_{EN} and C_{FB} capacitors Figure 1 & 2 updated in accordance. ASU & FB pin definitions updated in §5. Added in Table 3 of Section 6.2: $R_{TH(J-C)}$ In Table 6 of Section 6.4: Output Voltage Accuracy added, conditions updated. Updated in Table 7 of Section 6.5: Internal Thermal Shutdown Temperature, conditions. Updated in Section 8, Output Voltage Setting and Accuracy calculations. In section 10, figures updated.

Table 8: Revision history

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