DATASHEET

20-A POL

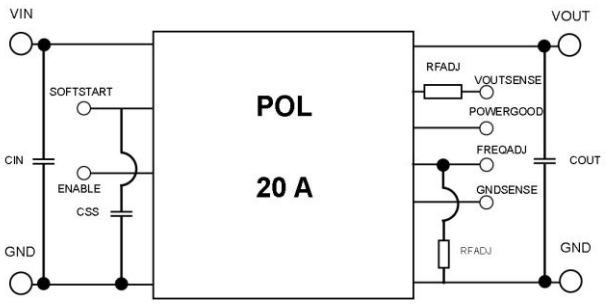
3DPM0602-1

Point-Of-Load, fully Integrated, Radiation Hardened by design

Image of the 3DPM0602 model. Actual markings may vary from those shown.

1. Features

- Radiation performance:
  - Radiation-hardness-assured up to TID 50 krad (Si)
  - SEL, SEB, and SEGR immune to LET = 62.5 MeV-cm^2 /mg
  - SET and SEFI characterized up to LET = 62.5 MeV-cm2 /mg
- Peak Efficiency 90%, full load efficiency above 80% (Vin = 12 V, Vout = 1 V, Iout =20 A)
- Low footprint (30 × 30 mm)
- Ultra-low profile (8 mm)
  High power density (>2.2 W/cm^3)
- Power rail: 4.6 V to 13.2 V on VIN
- Adjustable output voltage: 0.8 V to 3.3 V
- Up to 20-A Output current
- Protection:
  - Input Undervoltage Detection Protection
  - Output Short Circuit Protection
  - Internal Thermal Protection
- Input Enable Control
- Low Output Noise
- Adjustable Soft Start: from 1 to 20ms
- Radiation Hardened by design
- ITAR Free



Functional Diagram

2. Application

- Space satellite point of load supply: FPGA, CPLD, DSP, CPU core, and I/O voltages.

3. Description

The 3DPM0602-1 is a highly integrated synchronous buck Point-of-Load (POL) power module designed for demanding space applications. It supports a wide input voltage range from 4.6 V to 13.2 V and provides an adjustable output voltage from 0.8 V to 3.3 V, delivering up to 20-A output current (20-W maximum output power).

High-energy efficiency, reduced size, and a superior dynamic response are achieved through the incorporation of wide bandgap Gallium Nitride (GaN) components. The converter is engineered for high dynamic performance and ensures precise output voltage regulation, even under rapid load variations.

The 20-A POL converter provides full protection against output short-circuit conditions. It also includes input under-voltage protection (UVP) and thermal shutdown circuitry, which disables operation when the internal temperature of the power module exceeds its specified thermal limit. This robust and efficient design makes it ideally suited for advanced space applications requiring high reliability and dependable power delivery.

Device Information

PART NUMBER(1)	GRADE	PACKAGE
3DPM0602-1 IB	Industrial	30 × 30 × 8 mm^3 (2) SMD package with gull-wing leads Mass = 20g(3)
3DPM0602-1 SB		
3DPM0602-1 IS	Space	
3DPM0602-1 SS		

Table 1 ***Device Information***

(1) For additional information view the Table 10 Ordering Information.

(2) Dimension values are nominal.

(3) Mass is accurate to ±10%.

Website Product Link: 3DPM0602-1

Table of Contents

Tables and Figures

4. Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
20/01/2026	1.0	Initial Release
10/03/2026	2.0	Add Table and Figures §9. *Radiation* Performance: Update SEE specification *Table 7 Thermal Resistances*: Rename thermal resistances

Table 2 Revision history

5. Pin Configuration and Function

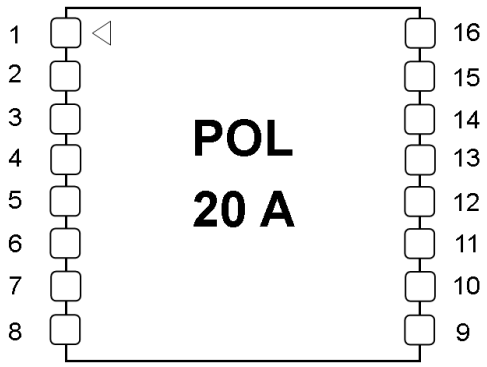


Figure 1 Top view 3DPM0602-1 Power module

PIN		I/O	DESCRIPTION
PIN #	PIN NAME		
1,2,10,11,12	GND	-	Ground associated with the internal analog control circuitry and power cell. Connect this pin directly to the PCB ground plane.
3,4	VIN	I	Input power. These pins shall be connected to a common supply rail within the 4.6-V to 13.2-V range.
5	FREQADJ	I/O	Frequency adjustment. The internal operating frequency is programmed by an external resistor connected between the FREQADJ pin and GND. The resistor value determines the operating frequency range; refer to the Description section for details.
6	POWERGOOD	O	Power-good output. This pin is an open drain logic output that is pulled to GND when the output voltage is outside a ±8% typical regulation window. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during soft start.
7	ENABLE	I	The ENABLE pin allows starting or stopping the converter via a logic input (TTL levels). A high logic level starts the converter, while a low logic level stops it. If not used, a pull-up resistor to Vin must be inserted (see Description section).
8	SOFTSTART	I/O	Soft-start pin. An external capacitor must be connected between the SOFTSTART pin and ground (GND) that sets the output voltage rise time.
9	GNDSENSE	I	Ground sense. The GNDSENSE pin shall be connected to the load return to ensure accurate output voltage regulation at the load. If unused, connect GNDSENSE to GND.
13,14,15	VOUT	O	Output power.
16	VOUTSENSE	I	The VOUTSENSE pin must be connected to the load supply to ensure that the output voltage regulation is as close as possible to the load. If not used, connect it to VOUT.

Table 3 Pin Description

6. Specifications

6.1 Absolute Maximum Ratings

PARAMETER		Min	Max	Unit
Input Voltage (vs GND)	VIN	-0.3	20	V
	FREQADJ	-0.3	6.5	
	SOFTSTART	-0.3	6.5	
	ENABLE	-0.3	6.5	
	POWERGOOD	-0.3	6.5	
	GNDSENSE	-0.3	6.5	
	VOUT	-0.3	6.5	
	VOUTSENSE	-0.3	6.5	
Vdiff	GND to GND Sense	-0.2	0.2	V
Source Current	POWERGOOD	±10		mA
	SOFTSTART	±10		
	FREQADJ	±10		
Sink Current	VIN	0.08	5.5	A
	ENABLE	200	500	µA
Operating junction temperature		-40	+125	°C
Storage temperature		-40	+150	°C

Table 4 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

Over operating temperature

			VALUE	UNIT
V_ESD	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±1000	

Table 5 ESD ratings

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

$T_J = -40°C$ to $+105°C$, 0 to 50 krad, $V_{in} = 4.6$ V to 13.2 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
VIN operating input voltage		4.6		13.2	V
VIN full performance input voltage	Transient performance and efficiency guaranteed for these input voltage values.	5		12	V
VIN operating supply current		0.08		5.5	A
VIN non-operating supply current	ENABLE = OFF	0.01		0.1	A
VIN input voltage ripple	Cin ≥ 60uF (external)	1		5(1)	%VIN
OUTPUT VOLTAGE AND CURRENT					
VOUT operating input voltage		0.8		3.3	V
VOUT supply current				20(2)	A
VOUT Regulation	VOUT < 1.5 V **BOL**(3)	-1.5		+1.5	%VOUT
	VOUT < 1.5 V **EOL**(4)	-2.1		+2.1	%VOUT
	VOUT ≥ 1.5 V **BOL**(3)	-1.8		+1.8	%VOUT
	VOUT ≥ 1.5 V **EOL**(4)	-2.5		+2.5	%VOUT
VOUT Voltage Ripple	Cout ≥ 220 µF (external)		1	2(5)	%VOUT
Load Regulation			0	0.2	%VOUT
VOUT Transient (output current transient)	Iout: 0→20 A, 1 A/µs(6)		5		%VOUT
	Iout: 20→0 A, 1 A/µs(6)		5		%VOUT
	Recovery Time(7)		150		µs
VOUT Transient (input voltage transient)	Vin transient ±10% in 1ms		2		%VOUT
POWER AND THERMAL PERFORMANCE					
Efficiency	IOUT > 2A	80		95	%
Losses	Internal power module losses	0.2		5.5	W
Internal Temperature	Junction Temperature (Internal)	-40		125	°C
ENABLE FUNCTION					
Input voltage	Input voltage on ENABLE INPUT pin to activate ENABLE input	3.85		13.2	V
ENABLE input current		45	55	60	µA
UVD PROTECTION					
VIN internal UVD threshold	VIN falling	4.15	4.27	4.38	V
	VIN rising	4.32	4.45	4.58	V
VIN internal UVD hysteresis		0.170	0.180	0.190	V
SHORT CIRCUIT PROTECTION					
Short Circuit Protection response time	ROUT Short Circuit ≤15 mΩ	1		15	µs
SOFT START					
SOFT START time	Without external capacitor Vout ≤ 1.5 V	750	1000	1250	µs
SOFT START time	With 2.2uF external capacitor, Vout > 1.5 V	3500	3800	4100	µs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL					
Switching Frequency	Vout ≤1.5 V	300	500	800	kHz
	Vout >1.5 V	300	500	1000	kHz
POWER GOOD SIGNAL					
Rising threshold (8)	Vout = [0.8; 3.3] V	-8	-5.0	-2.5	%VOUT
Falling Threshold (8)	Vout = [0.8; 3.3] V	+2.5	+5.0	+8	
POWERGOOD source current	Power good signal pin output current (9)			500	µA
POWERGOOD Voltage	Power good signal pin output voltage for 1µA Source Current	3.9	4.5	5.28	V
	Power Good Source Impedance		3.5		kΩ
	Power Good Sink Impedance		13.3		
OVER TEMPERATURE PROTECTION					
Over temperature protection threshold	Internal temperature	126	135	149	°C

Table 6 Recommended Operating Conditions

(1) With a minimum of 60 µF additional input capacitor
(2) For Vout ≤ 1 V at 85°C, the maximum output current (20 A) applies. For Vout > 1 V at 85°C, Iout max = 20 W / Vout. For 105°C, refer to the thermal information in Section 6.5 for the maximum allowable current.
(3) Begin of Life Performance
(4) End of Life performance includes aging and radiation degradation.
(5) With a minimum of 220 µF additional output capacitor
(6) For Vout = [0.8 ; 3.3] V
(7) Time for output voltage to settle within 2% of steady-state value.
(8) The Power Good (PG) signal is asserted and deasserted based on the output voltage level relative to the nominal VOUT. The rising and falling thresholds are expressed as a percentage of VOUT and define the Power Good hysteresis window.
(9) Maximum source current on the Power Good pin while maintaining TTL 5 V logic compatibility (minimum high-level output voltage ≥ 2.1 V).

6.4 Typical Characteristics

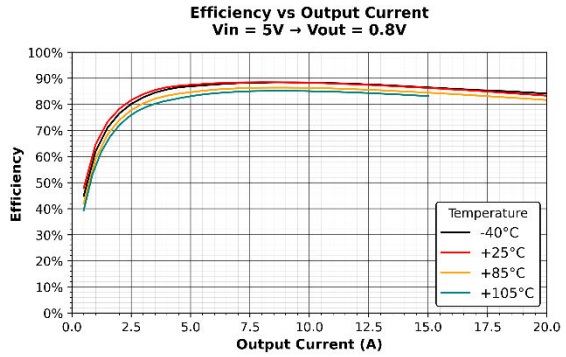


Figure 2 Efficiency for VIN = 5 V, VOUT = 0.8V

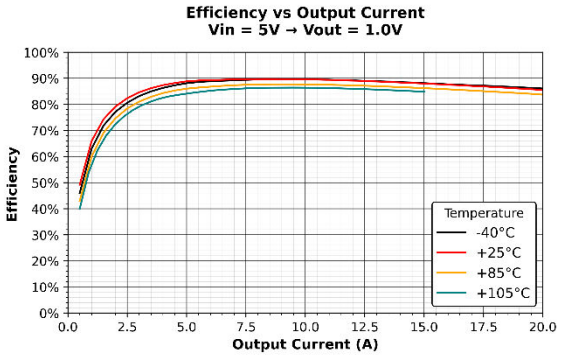


Figure 3 Efficiency for VIN = 5 V, VOUT = 1.0V

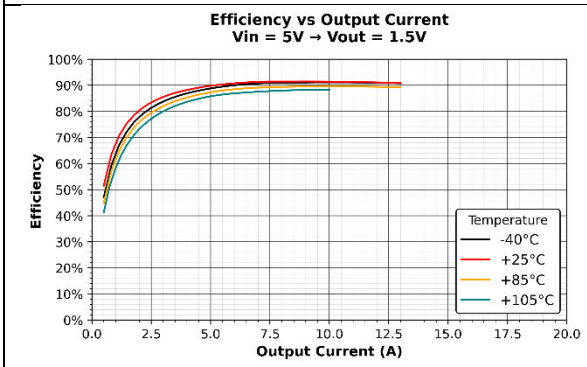


Figure 4 Efficiency for VIN = 5 V, VOUT = 1.5V

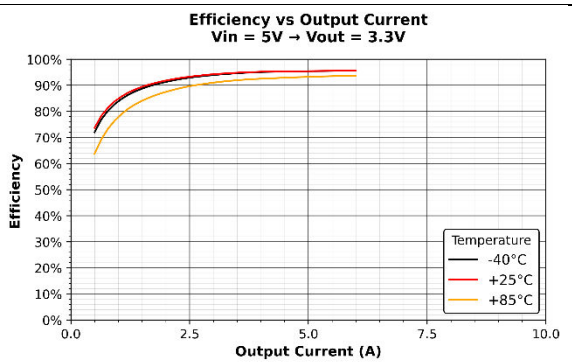


Figure 5 Efficiency for VIN = 5 V, VOUT = 3.3V

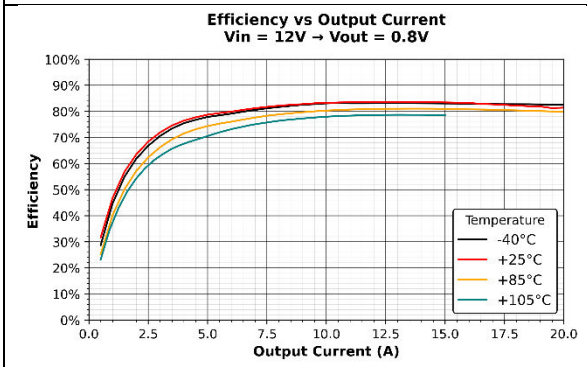


Figure 6 Efficiency for VIN = 12 V, VOUT = 0.8V

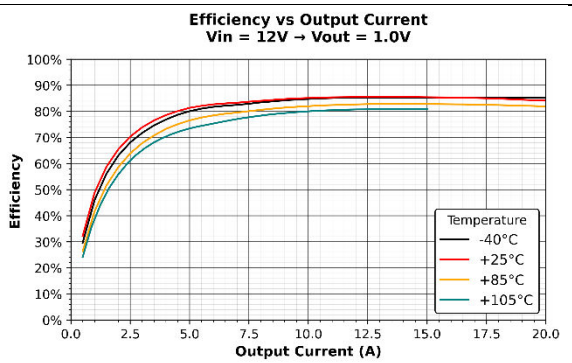


Figure 7 Efficiency for VIN = 12 V, VOUT = 1.0V

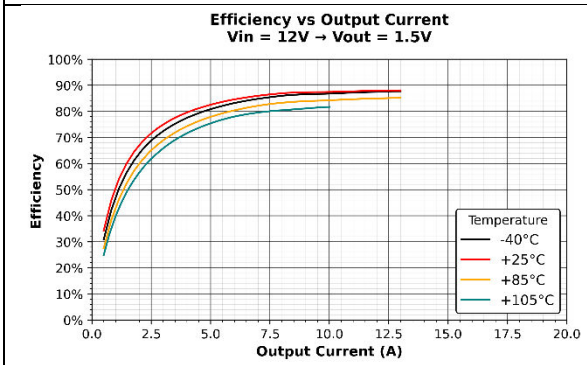


Figure 8 Efficiency for VIN = 12 V, VOUT = 1.5V

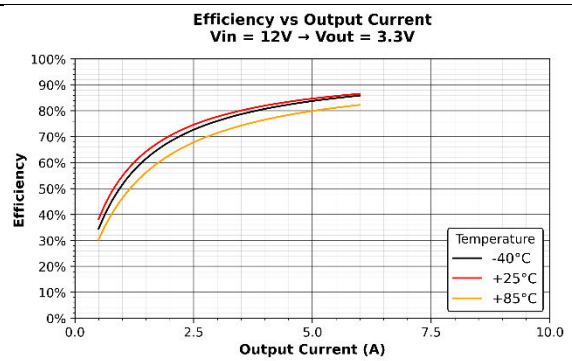


Figure 9 Efficiency for VIN = 12 V, VOUT = 3.3V

6.5 Thermal Information

6.5.1 Thermal Resistance Data

The thermal simulations were performed for a vacuum-like environment such as outer space.

THERMAL resistance		VALUE	UNIT
$R_{th(J-A)}$	Junction-to-Ambiant (1) thermal resistance (without underfill)	**15**	**°C/W**
$R_{th(J-A\_u)}$	Junction-to-Ambiant (2) thermal resistance (with underfill)	**5**	**°C/W**

Table 7 Thermal Resistances

(1) In Rth(J-A) (Junction-to-Ambiant thermal resistance), Ambiant is defined as the temperature at the bottom of the leads in contact with the board, Junction represents the temperature of the internal hottest die of the module. This value is obtained by simulation.

(2) In Rth(J-A_u) (Thermal resistance Junction to Ambient with underfill), Ambient is defined as the hottest temperature under the underfill/leads in contact with the board, Junction represents the temperature of the internal hottest die of the module. This value is obtained by simulation

6.5.2 Thermal Management and Mounting Requirements

To achieve the full rated performance of the 20-A POL module, an optimal thermal coupling between the module's bottom surface and the host PCB is mandatory.

- Attachment Process: It is strongly recommended to bond the module to the host PCB using a high-conductivity thermal interface material (TIM) prior to the manual soldering of electrical connections.
- Recommended Material: Use a thermal adhesive with a minimum thermal conductivity of 1.44W/(m·K), such as *LOCTITE ABLESTIK 285 CAT 9*.
- Application Profile: Apply approximately 0.7 g (±0.1 g) of adhesive in a cross pattern with a diameter of 26 mm.

If you don't use the recommended bonding process significantly increases thermal resistance and requires immediate power derating as defined in Section 6.5.3.

6.5.3 Power Derating and Operating Limits

6.5.3.1 Non-Attached Configuration (Solder Only)

If the module is mounted using only electrical solder joints without thermal adhesive, the following operating constraints apply to prevent thermal runaway:

- Output Voltage Range: Limited to 0.8 V ≤ Vout ≤ 1.5 V
- Maximum Power/Current: Limited to 15 A or 15 W, whichever limit is reached first.

6.5.3.2 Thermal Derating Curve (Standard Configuration)

To maintain the internal power dissipation of the 20-A POL module below the 5.5-W maximum limit, output current derating must be applied based on the temperature of the host PCB (T_{PCB}) on which the module is mounted:

- $T_{PCB} \leq 85°C$: Full rated output current (100% of IOUT) is available.
- $85°C \leq T_{PCB} \leq 105°C$: For configurations where Vout ≤ 1.5V the maximum output current decreases linearly from 100% to 75% of the nominal value.

- Maximum Operating Temperature: Operation at a PCB temperature exceeding 105°C is not supported and may lead to permanent device failure.

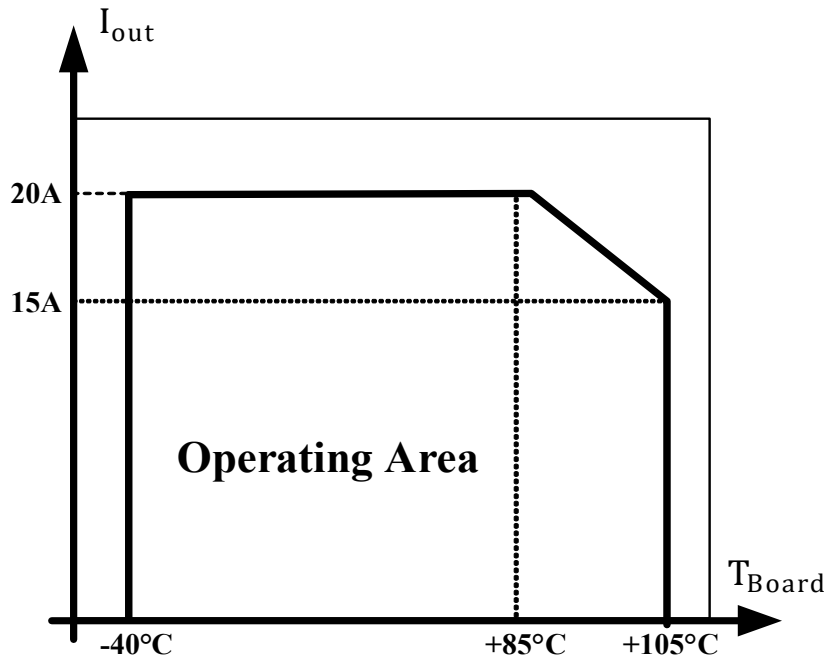


Figure 10 Output Current as a Function of Board Operating Temperature for VOUT ≤ 1 V (Module Attached to PCB Using Epoxy Adhesive)

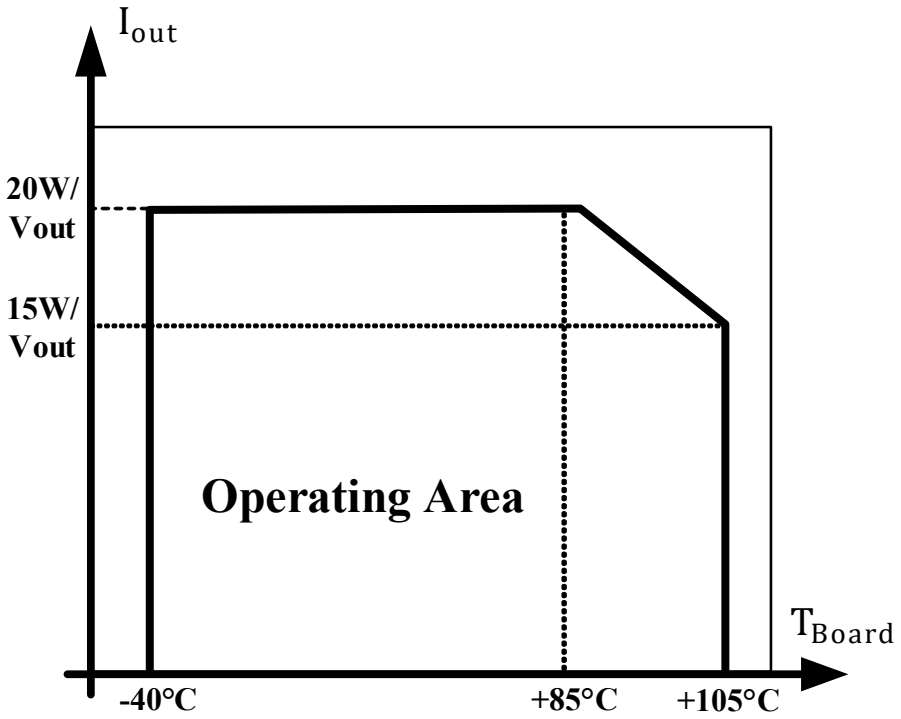


Figure 11 Output Current as a Function of Board Operating Temperature for 1 V < Vout ≤ 1.5 V (Module Attached to PCB Using Epoxy Adhesive)

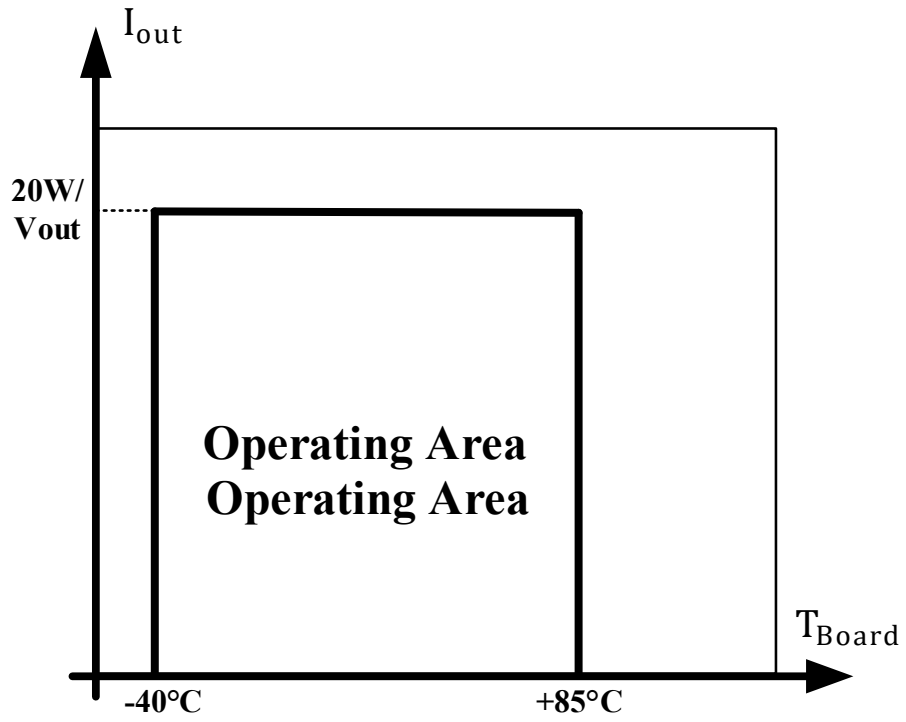


Figure 12 Output Current as a Function of Board Operating Temperature for Vout > 1.5 V (Module Attached to PCB Using Epoxy Adhesive)

7. Detailed Description

7.1 Overview

The 20-A POL is a GaN-based synchronous step-down (buck) converter designed for high-current, low-voltage point-of-load applications. Both high-side and low-side switches are GaN transistors, with the low-side path optimized to reduce conduction losses at low duty cycles. A diode across the low-side switches mitigates dead-time losses, ensuring efficient operation at high switching frequency.

Voltage Regulation: The 20-A POL uses a hysteretic with Constant-On-Time (COT) control scheme with an internal noise injection, enabling fast and stable output voltage regulation. A secondary integrator loop corrects static errors, ensuring precise output voltage under different load and input conditions. This architecture provides excellent transient response while maintaining unconditional stability.

Soft-Start and Sequencing: The device implements a controlled soft-start, ramping the output voltage gradually to minimize inrush currents and prevent overshoot during power-up.

Undervoltage Protection: The 20-A POL continuously monitors the input voltage. If the voltage drops below a defined threshold, both high-side and low-side switches are disabled to prevent operation under unsafe conditions, ensuring reliable startup and shutdown behavior.

Output Current Short-Circuit Protection: Integrated current sensing detects VOUT–GND short circuits (≤15 mΩ). On detection, the converter immediately stops switching and latches off, protecting both the module and the upstream power supply.

Over-Temperature Protection: The device continuously monitors the internal hot spot PCB temperature. If it exceeds a defined safe limit, the converter shuts down to prevent damage. Operation automatically resumes when the temperature returns to safe levels.

Power-Good Indicator: A dedicated signal pin provides feedback on output voltage status, allowing the system to detect when the output is within the specified regulation range.

Performance: The 20-A POL delivers up to 20 A of continuous output current with rapid transient response (<50 µs for full-load steps) and high efficiency (80–95%). Its combination of fast GaN switching, optimized low-impedance power stage, advanced voltage regulation, and comprehensive protection makes it ideal for modern computing, AI workloads, and other high-performance point-of-load applications.

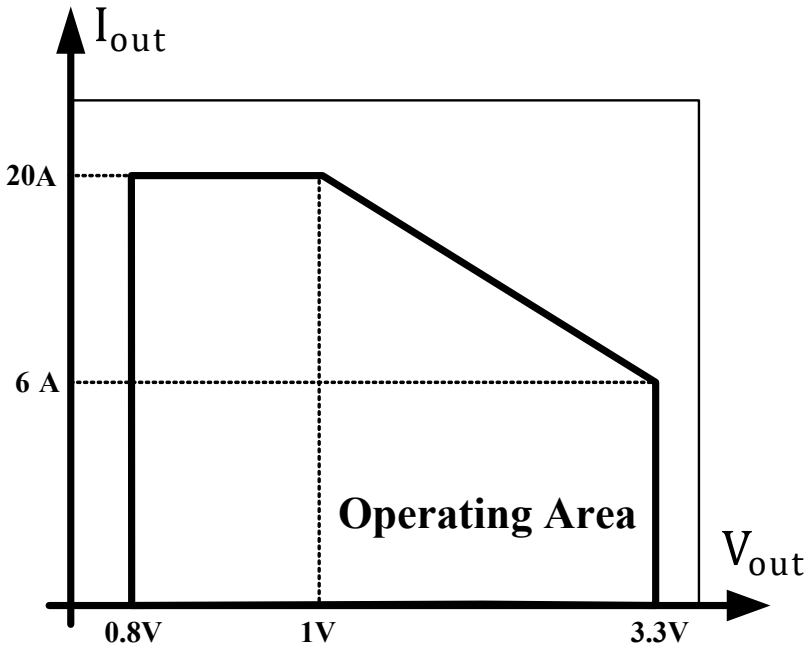


Figure 13 Output Current as a Function of Operating Output Voltage

7.2 Functional Block Diagram

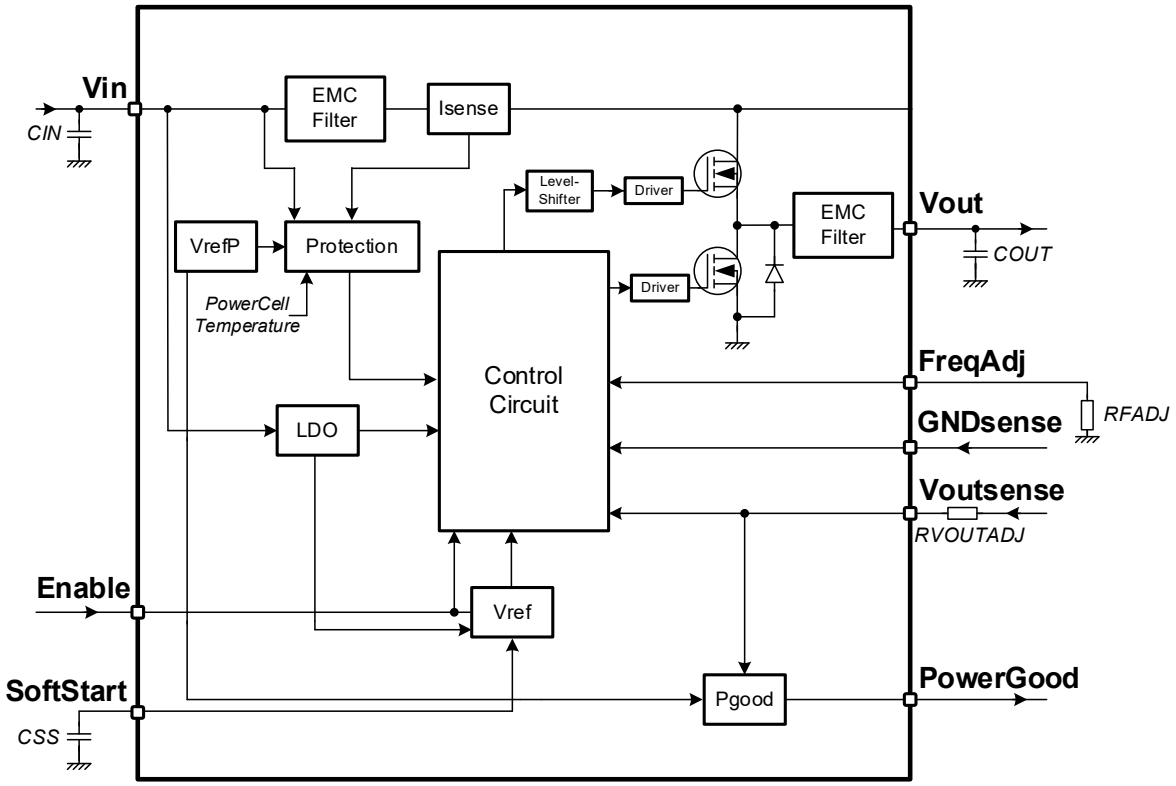


Figure 14 Functional Block Diagram

7.3 Feature Description

7.3.1 Converter Input

The 3DPM0602-1 converter includes internal input capacitance within the power module. However, to guarantee the performance specified in Section 6.3, it is necessary to add a minimum of 60 µF of external tantalum capacitance at end-of-life conditions.

To ensure this value, two 35 V, 47 µF T591X476M035ATE075 (or equivalent) tantalum capacitors are recommended. These capacitors should be placed as close as possible to the module input, between the VIN and GND pins.

7.3.2 Converter Output

The 3DPM0602-1 converter includes internal output capacitance within the power module. However, to guarantee the performance specified in Section 6.3, it is necessary to add a minimum of 220 µF of external tantalum capacitance at the module output (worst-case end-of-life value).

To achieve this, one 10 V, 330 µF T530X337M010AHE004 (or equivalent) tantalum capacitor is recommended. The ESR of this capacitor, or any external capacitors placed in parallel with the module, must be less than or equal to 4 mΩ to ensure proper dynamic performance.

If higher performance than specified is required for your application, it is advisable to add additional output capacitors in parallel to reduce the ESR while increasing the total capacitance. It is important to note that the PCB layout on which the POL module is soldered plays a critical role in transient performance. Please refer to the dedicated PCB layout section in this datasheet.

7.3.3 Adjusting Output Voltage

The output voltage can be adjusted using a series resistor connected between the VOUT point where you want to regulate the voltage and the VoutSense pin of the module. The value of the resistor, depending on the desired output voltage (V_{out}), is given by the following formula:

$$R_{Vout,ADJ} = 330 \times \left(\frac{V_{out}}{0.6} - 1\right)$$

This resistor directly affects the accuracy of the target output voltage. To remain within the specifications of the datasheet, use a precision resistor (at least 0.1% tolerance or better) with a low temperature coefficient (at least 25 ppm/°C or better).

7.3.4 Adjusting Frequency

The converter uses a non-linear (voltage-hysteretic) control architecture with a constant on-time. Therefore, the conduction time of the high-side GaN transistor (Ton) must be adjusted according to the operating point (VIN and VOUT) to ensure that the switching frequency remains within the specified range.

The value of the R_FREQ_ADJ resistor connected to the corresponding pin is determined using one of two equations given below, selected according to the application output-voltage range. For convenience, typical resistor values calculated from these equations are provided in the table below (Table 7.3.4-1). These values are derived directly from the formulas.

If the selected resistor matches the calculated value within ±2.5%, the converter switching frequency will remain within the specified limits.

Any deviation greater than ±2.5% between the resistor value calculated using the formula and the resistor implemented will result in a proportional shift in the switching-frequency range. The frequency limits shown in the tables correspond to worst-case end-of-life (EOL) conditions, assuming an input-voltage range from 4.6 V to 13.2 V.

Case 1: Vout ≤ 1.5 V:

$$\mathbf{R_{user} = a \times T_{on} + b \times T_{on}^{\,2} + \frac{c}{V_{in}} + \frac{d \times T_{on}}{V_{in}} + e}$$

with $T_{on} = \frac{V_{out}}{V_{in}} \times 2500$

Coefficients :

- $a = 19.8$
- $b = 0.0184$
- $c = 5380$
- $d = -16.1$
- $e = -235$

Case 2: Vout > 1.5 V:

$$\mathbf{R_{user} = a \times T_{on} + b \times T_{on}^{\,2} + c \times V_{in} + d \times T_{on} \times V_{in} + e}$$

$$\mathbf{Maximal\ R_{Freq\_ADj} = 43200\Omega}$$

$$T_{on} = \min\left(\frac{V_{out}}{V_{in}} \times 2000\ ;\ 1111\right)$$

Coefficients :

- $a = 26.7$
- $b = 0.0156$
- $c = 422$
- $d = -0.641$
- $e = -4770$

For this operating range (Vout > 1.5 V), proper converter operation requires limiting the maximum resistor value. The R_FREQ_ADJ resistor must not exceed 43,2kΩ.

Pre-computed R_user Value Table

VIN (V)	VOUT (V)	Ton (ns)	R_User(Ω) (Formula)	R_FREQ_ADJ (Ω) (Recommended)
Vout ≤ 1.5 V				
5	0.8	400	10 417	10 500
5	1.0	500	13 731	14 000
5	1.2	600	17 413	17 800
5	1.5	750	23 626	23 700
12	0.8	166.7	3 801	3 830
12	1.0	208.3	4 857	4 870
12	1.2	250	5 978	5 900
12	1.5	312.5	7 778	7 870
Vout > 1.5 V				
5	1.8	720	22 343	22 600
5	2.0	800	26 120	26 100
5	2.5	1 000	36 435	36 500
5	3.3	1 111	43 200	42 200
12	1.8	300	7 400	7 500
12	2.0	333.3	8 363	8 250
12	2.5	416.7	10 922	11 000
12	3.3	550	15 467	15 400

Table 8 Precomputed R_FREQ_ADJ Resistance Values Based on Usage Configuration

7.3.5 Adjusting Output Voltage Soft Start

The output voltage rise time during converter startup (either via the ramp-up of Vin or by enabling the module through the ENABLE pin) is determined by the rise time of the internal voltage reference. This internal reference charges a capacitor at startup; the internal capacitance is 440 nF.

The rise time can be increased by adding an external capacitor between the SOFTSTART pin and ground (GND). The output voltage rise time to reach ±2% of its final value, as a function of the external capacitance Cext, is then given by the following equation:

$$V_{out}, TR_{2\%}(ns) = A + B \times C_{ext}$$

$$\Leftrightarrow C_{ext} = \frac{V_{out}, TR_{2\%} - A}{B}$$

With :

- A = 1045.52
- B = 1.3377
- C_{ext} in nF
- $V_{out}, TR_{2\%}$ in ns

For output voltages above 1.5 V, it is essential to add a minimum of 2.2 µF of external capacitance (Cext) to ensure that the output voltage does not exceed its final value during startup. The external capacitor (C_{ext}) is connected between the Soft Start (SS) pin and ground (GND). The voltage across Cext will not exceed 0.6 V under normal operation.

7.3.6 Under Voltage Detection Protection (UVD)

The undervoltage protection ensures that no commands are sent to the transistors when the input voltage is too low, guaranteeing optimal operation. This internal converter protection is not adjustable and ensures proper functioning across the entire input voltage range, regardless of the operating point. It also prevents voltage overshoot during startup or shutdown.

When this protection is activated, both the high-side and low-side GaN transistors are turned off.

7.3.7 Output current short circuit protection

The converter features an integrated, high-speed short-circuit protection (SCP) circuit designed to detect low-impedance faults. By continuously monitoring the current through the high-side GaN transistor, the device can identify short-circuit conditions where the output impedance is 15mΩ or less. Upon detection of such a fault, both the high-side and low-side transistors are immediately disabled. This rapid response safeguards the converter and the GaN power stage against potentially destructive output current transients.

This protection has a very high bandwidth (>1 MHz), allowing it to rapidly protect both the converter and the upstream bus. Its operation is as follows:

When a short circuit is detected, the converter commands are disabled for a duration between 4.5 µs and 11 µs (EOL, worst-case analysis). After this interval, the converter resumes regulation. If the short circuit persists, the protection immediately disables the commands again for the same duration. After 2 to 10 such interruptions, the converter shuts down permanently.

During these interruptions, it is guaranteed that no overshoot occurs at the converter output, preventing damage to the powered load.

To clear the fault, two options are available:

1. Power-cycle the converter by turning Vin off and on, or
2. Apply a low logic level for at least 10ms on the ENABLE pin, then return it high to restart the converter.

Then, the converter restarts. If the fault persists, the protection will immediately reactivate.

7.3.8 Over Temperature Protection

The internal thermal protection of the module is implemented using a thermistor, soldered as close as possible to the components that dissipate the most power within the core of the power cell.

The purpose of this protection is to prevent converter destruction in case of overheating of the power cell elements. This overheating may occur when the operating temperature exceeds the specified maximum rating (+85°C or +105°C depending on configuration).

7.3.9 Power Good signal

The Power Good signal indicates when the output voltage is within ±8% (worst-case EOL) of its nominal value.

When this condition is met, the Power Good signal switches to a logic high state.

- Logic high level: between 4 V and 5.35 V (with source current ≤ 1 µA)
- Logic low level: between 0 V and 100 mV (with source current ≤ 1 µA)
- PowerGood Pin source impedance: 3.5 kΩ
- PowerGood Pin sink impedance: 13.3 kΩ

If the drawn current exceeds 500 µA, the logic high voltage level is no longer guaranteed; however, the converter functionality remains unaffected.

The Power-Good (PGOOD) signal exhibits a startup response time of up to 6ms, depending on the VIN ramp-up time. Once the converter is in steady-state operation, the PGOOD response time is approximately 40µs.

This Power Good signal can be used either to detect the triggering of an internal protection or to provide sequencing between multiple POL converters.

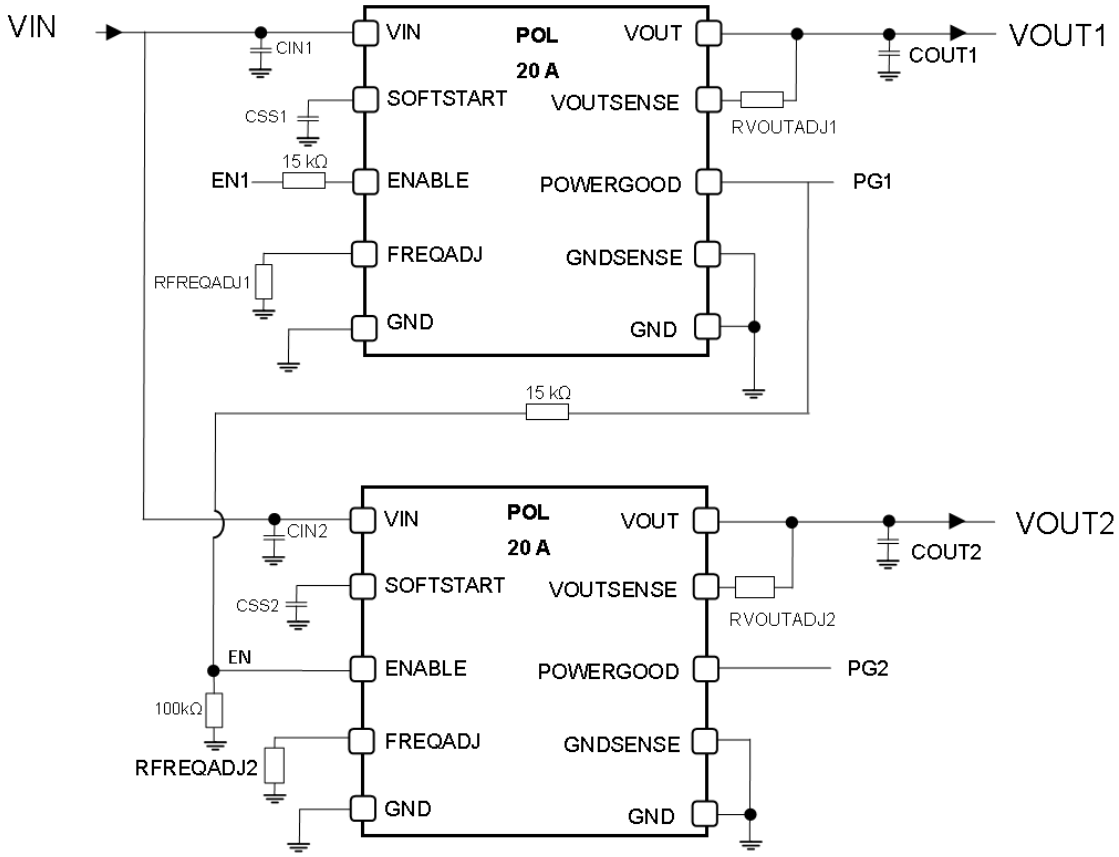
7.3.10 Input Enable and Sequencing

The INPUT ENABLE pin on the converter allows starting or stopping the converter via a logic input.

- Logic high level (input): 3.85 V (min) to 13.2 V (max). An external 15 kΩ series resistor is required for this input.
- Automatic Startup Configuration: If the enable function is not required, connect a 15 kΩ pull-up resistor between VIN and the INPUT ENABLE pin. In this "always-on" configuration, the converter will automatically initiate startup once VIN exceeds the 4.6 V UVP threshold.

When this pin is used to start/stop the converter, each startup follows the output voltage ramp defined by the soft-start mechanism (see Soft Start section). During shutdown (INPUT ENABLE = 0), both transistors (high-side and low-side) are turned off, leaving the output floating.

This pin can also be used to sequence multiple POL converters. For example, connect the POWER GOOD pin of POL #1 to the INPUT ENABLE pin of POL #2. POL #2 will then start once the output of POL #1 is stable. This method can be extended to sequence as many POLs as needed.



wFigure 15 Example of using two 20-A POL converters with sequential startup.

When the output voltage of POL No. 1 (the upper one) reaches its final value, POL No. 2 then starts in turn. The same sequence applies during shutdown.

8. Application and Implementation

Note

The information provided in the following Applications sections is not part of the official 3D PLUS component specifications, and 3D PLUS does not guarantee its accuracy or completeness. Customers are responsible for determining the suitability of components for their applications and should validate and test their designs to ensure proper system functionality.

8.1 Application Information

The 3DPM0602-1 device is a highly integrated synchronous step-down DC-DC converter. It converts a higher DC input voltage to a lower DC output voltage with a maximum output current of 20 A (subject to temperature derating).

8.2 Typical Application

The following application scenario represents a typical high-performance configuration for this Point-of-Load (PoL) converter, converting a 12-V input rail to a 1V output for high-current digital loads. This setup utilizes a 10-µF soft-start capacitor to achieve a controlled monotonic power-up ramp of approximately 14ms, effectively limiting inrush current. The input filter consists of two 47-µF capacitors and a 30-V Tantalum capacitor (ref: T591X476M035ATE075) to provide a low-impedance source for the GaN power stage. To ensure minimal output voltage ripple and superior transient response, a single 330-µF Tantalum output capacitor (ref: T530X337M010AHE004) with a low ESR of 4 mΩ is employed.

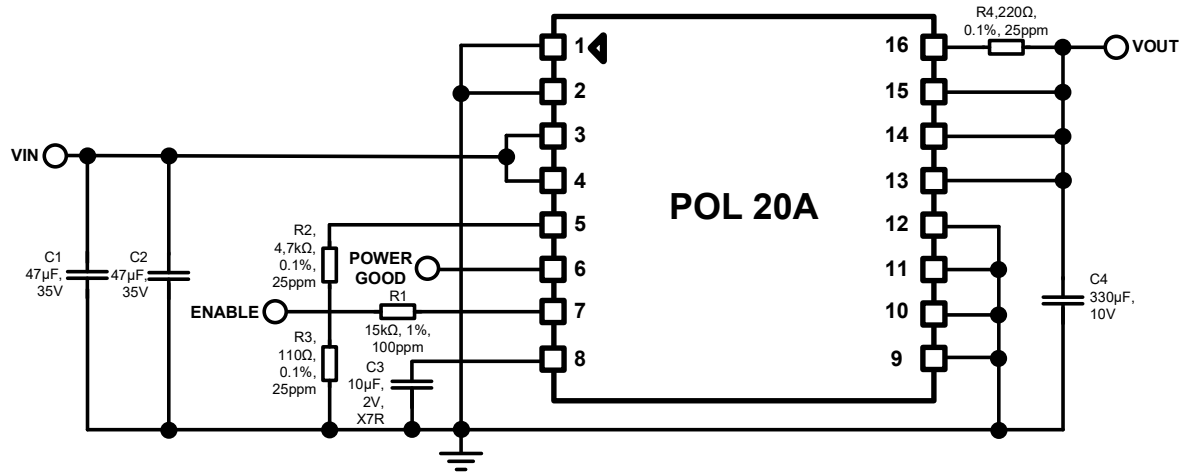


Figure 16 Schematic of the 20-A POL wired in the configuration shown in this application example

Design Parameters and Component Configuration:

Design Parameter	Value
Input Voltage	12 V ±10%
Output Voltage	1 V
Output Current	Max 20 A (T = 85°C)
Soft-Start Capacitance	10 µF, 4V, 0805ZC106K4T2A (Vout Start in 14 ms)
RFADJ Config Resistor	4810 Ω (4.7 kΩ + 110 Ω, 0.1%, 25ppm)
Vout Config Resistor	220 Ω, 0.1%, 25 ppm
Input Capacitance	2x 47 µF, 35 V, T591X476M035ATE075
Output Capacitance	1x 330 µF T530X337M010AHE004
Load Transient Slew Rate	1 A/µs

Table 9 Proposed Designed Parameter Values

Typical Performance Characteristics

Full-Load Start-up Sequence: The converter's start-up behavior is evaluated under a constant 20-A load. Figure 17 Start-up Waveform – Vin, Vout, PGOOD, UVD illustrates the timing relationship between the input voltage (VIN) the output voltage (VOUT), and the digital diagnostic signals: Power Good (PGOOD) and Under-Voltage Detection (UVD). The soft-start mechanism ensures a smooth transition to regulation without overshoot.

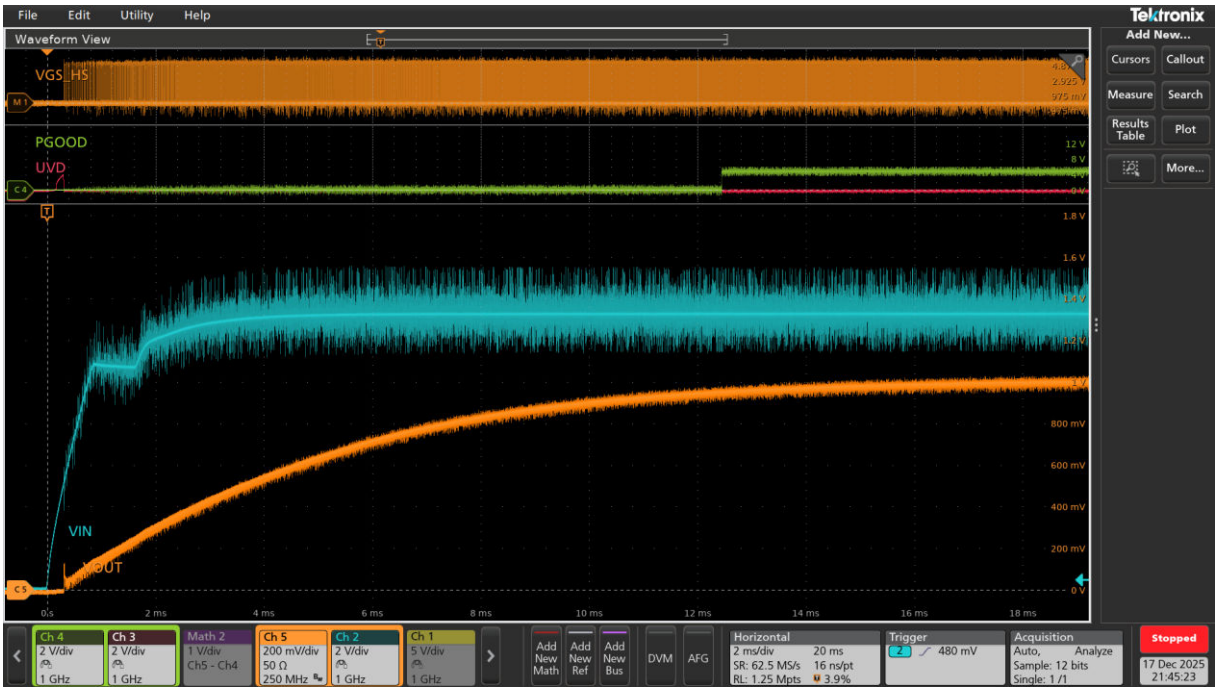


Figure 17 Start-up Waveform – Vin, Vout, PGOOD, UVD

Static Output Ripple: The steady-state output voltage ripple is characterized at both no-load (0 A) and full-rated load (20 A). Due to the high switching frequency and the 4-mΩ ESR of the output capacitor, the ripple remains within tight tolerances across the entire load range (±1.8%).

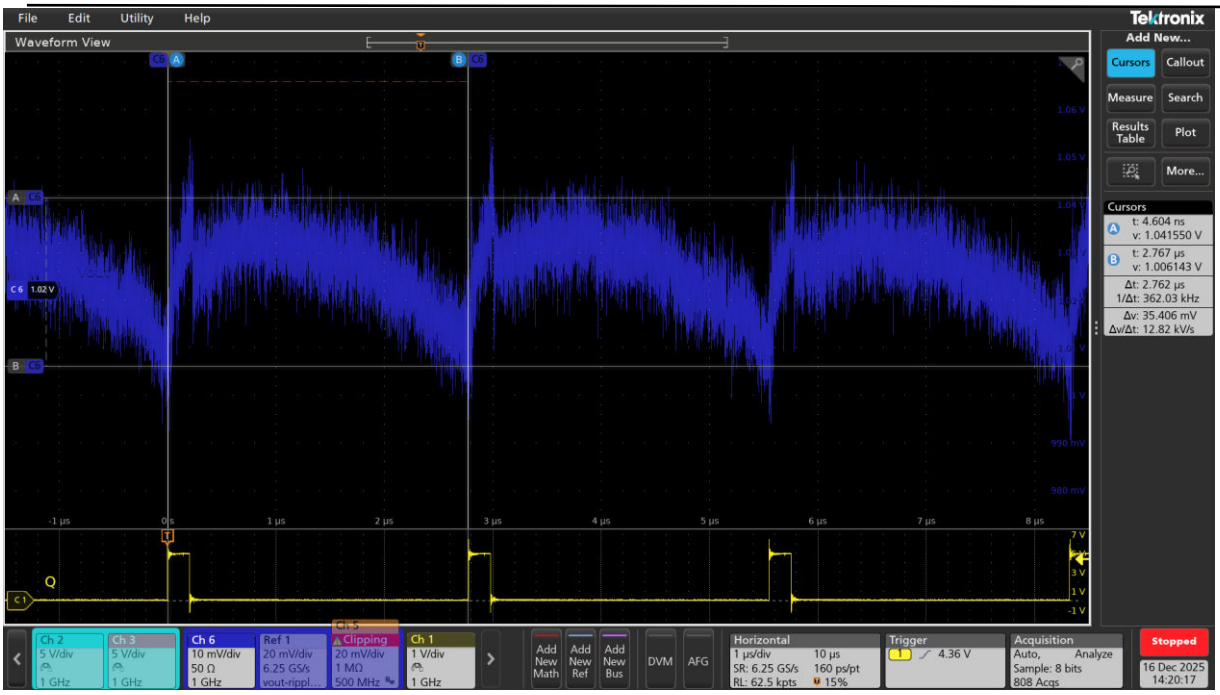


Figure 18 Output Voltage Steady-State Ripple at Iout = 0 A

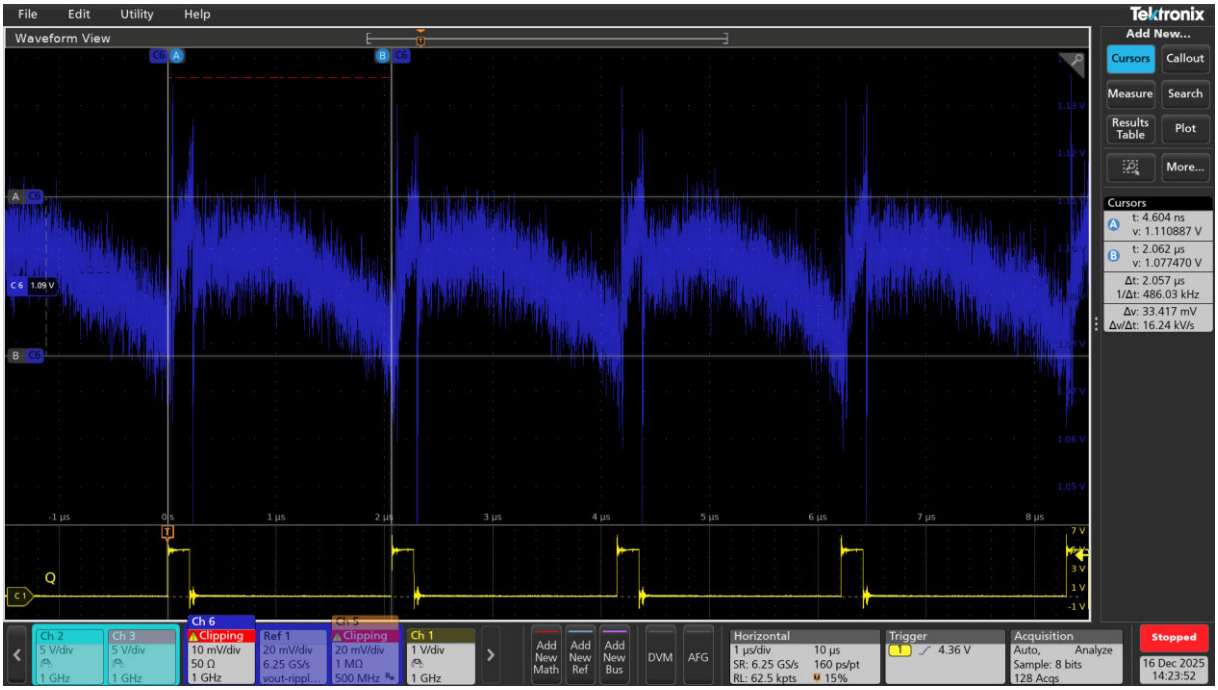


Figure 19 Output Voltage Steady-State Ripple at Iout = 20 A

Load Transient Response: The dynamic performance is verified using a high di/dt load step. Figure 20 displays the output voltage deviation during a 0-A to 20-A step at a 1 A/µs slew rate.

Conversely, Figure 21 shows the response during a load release (20 A to 0 A). The low-impedance GaN stage and optimized control loop ensure rapid recovery with minimal under-shoot and over-shoot.

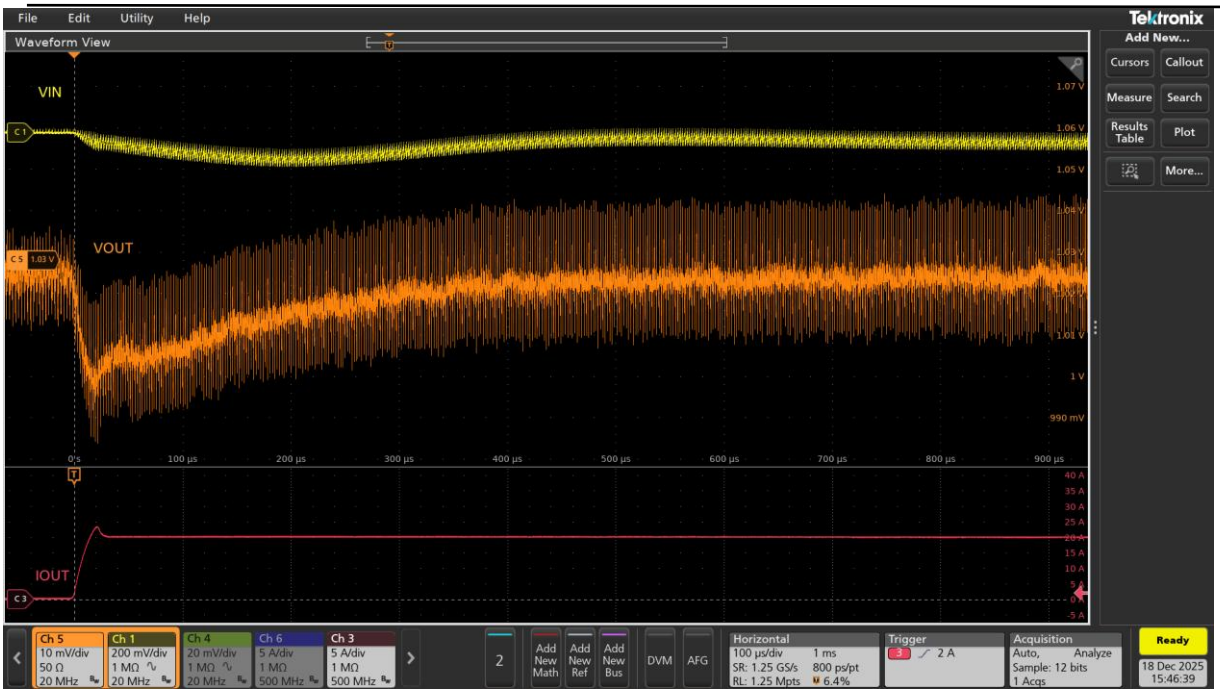


Figure 20 Load Step 0 A to 20 A, 1 A/us

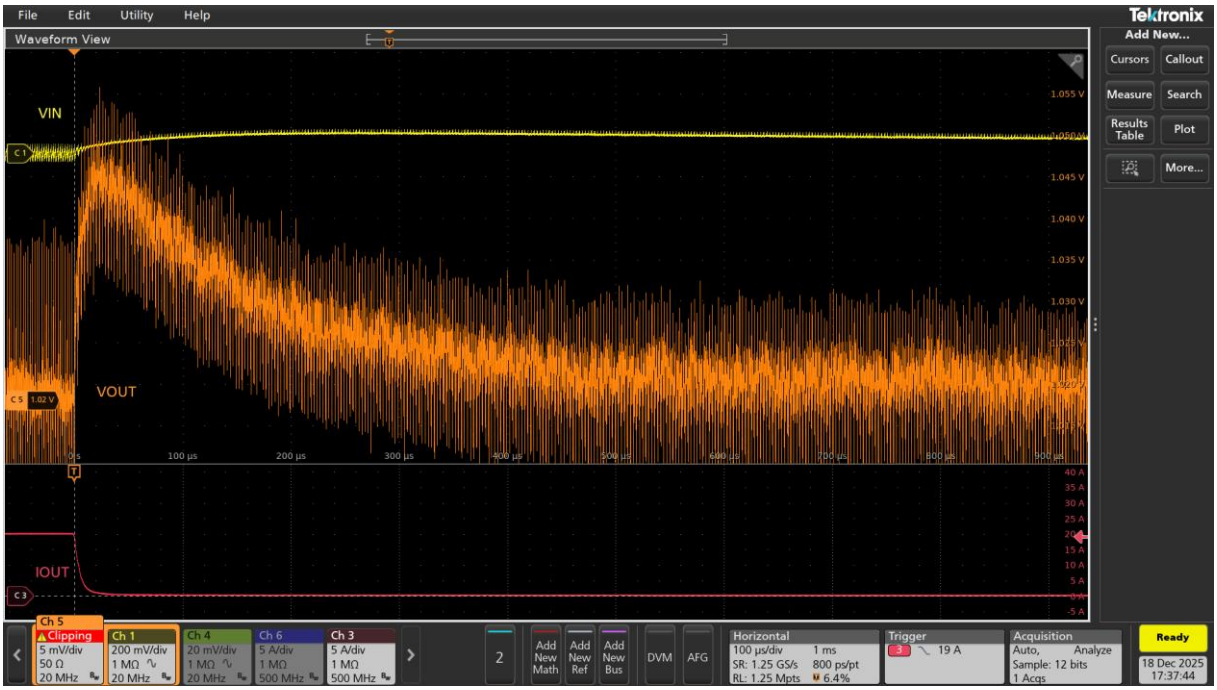


Figure 21 Load Drop 20 A to 0 A, 1 A/us

8.3 Power Supply Recommendations

The 3DPM0602-1 is designed to operate from an input voltage supply range between 4.6 V to 13.2 V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 60 µF (after de-rating) tantalum capacitor or better from VIN to GND.

Additional capacitors may be required in systems with small input ripple specifications (less than 5%), as well as if the 3DPM0602-1 device is located more than a few centimeters away from its input power supply.

8.4 Layout Recommendations

PCB layout is a critical aspect of good power supply design. Refer to the Layout Example section for a sample PCB layout.

Key recommendations:

- Include a large top-layer ground area. Connect this area to internal ground layers using vias near the input bypass capacitor, output filter capacitor, and directly under the 3DPM0602-1 module to provide a thermal path from the exposed pad to ground. For full-load operation, the top-layer ground and internal planes must provide sufficient heat dissipation.
- Tie the GND pin directly to the thermal pad under the module.
- High-speed signal paths can interact with stray inductance or parasitic capacitance, generating noise or degrading performance. Bypass the VIN pin to ground using a low-ESR tantalum capacitor (or X7R ceramic with sufficient value). Minimize the loop area formed by the bypass capacitor, VIN pins, and ground connections.
- The output filter capacitor ground should share the same power ground trace as the VIN bypass capacitor. Keep these traces as short and wide as possible.
- Route feedback traces away from inductor EMI and noisy power traces. Avoid placing feedback traces directly under the Vout plane. If unavoidable, route them on a separate layer with a ground plane between the trace and the inductor.
- Keep resistors used for VSENSE as close to the device pins as possible to reduce noise pickup.
- Make all high-current traces as short, direct, and wide as possible.

Alternative PCB layouts may achieve acceptable performance, but this approach has been validated and serves as a recommended guideline.

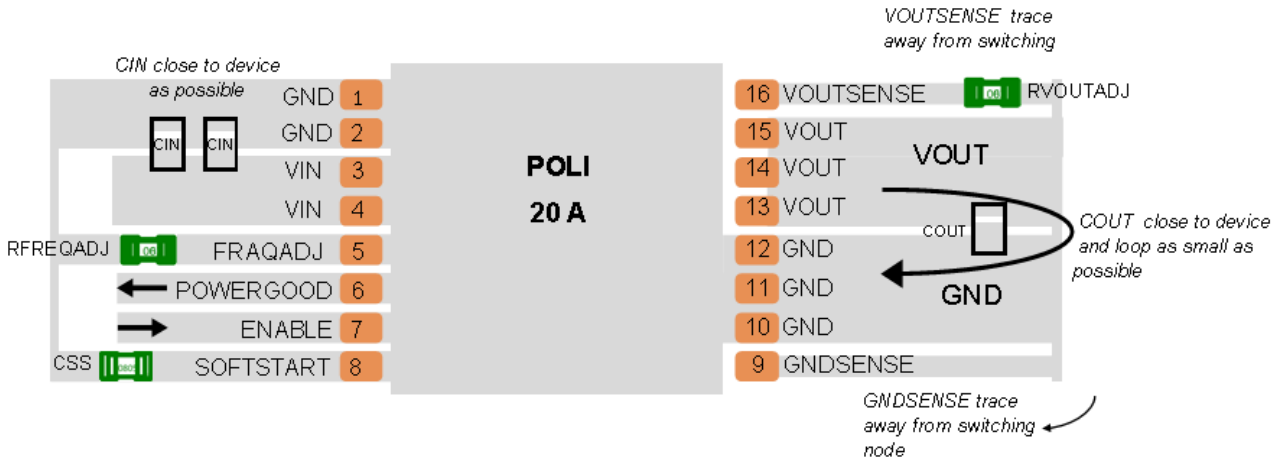


Figure 22 Recommanded layout for 20-A POL power module

8.5 Soldering Recommendations

To ensure mechanical integrity and prevent thermal damage to internal components, the **20-A POL** module should be assembled using manual soldering. The following guidelines must be observed:

- **Maximum Iron Tip Temperature:** 280°C.
- **Maximum Dwell Time at +280°C:** 40 seconds per terminal.
- **Soldering Sequence:** It is highly recommended to solder the pins in a **staggered (cross-pattern) sequence** to ensure uniform heat distribution across the module (*Example sequence:* Pin 1, then Pin 9, followed by Pin 2, then Pin 10…).

9. Radiation Performance

The 3DPM0602-1 is qualified for space flight applications and is Radiation Hardness Assured (RHA) up to a Total Ionizing Dose (TID) of 50 krad(Si). Regarding Single Event Effects (SEE), the module is immune to Single Event Latch-up (SEL), Single Event Burn-out (SEB), and Single Event Gate Rupture (SEGR) up to a Linear Energy Transfer (LET) of 62.5 MeV·cm^2/mg. Additionally, Single Event Transients (SET) and Single Event Functional Interrupts (SEFI) are fully characterized up to the same LET threshold of 62.5 MeV·cm^2/mg.

10. Mechanical and Packaging

10.1 Package Outline Drawings

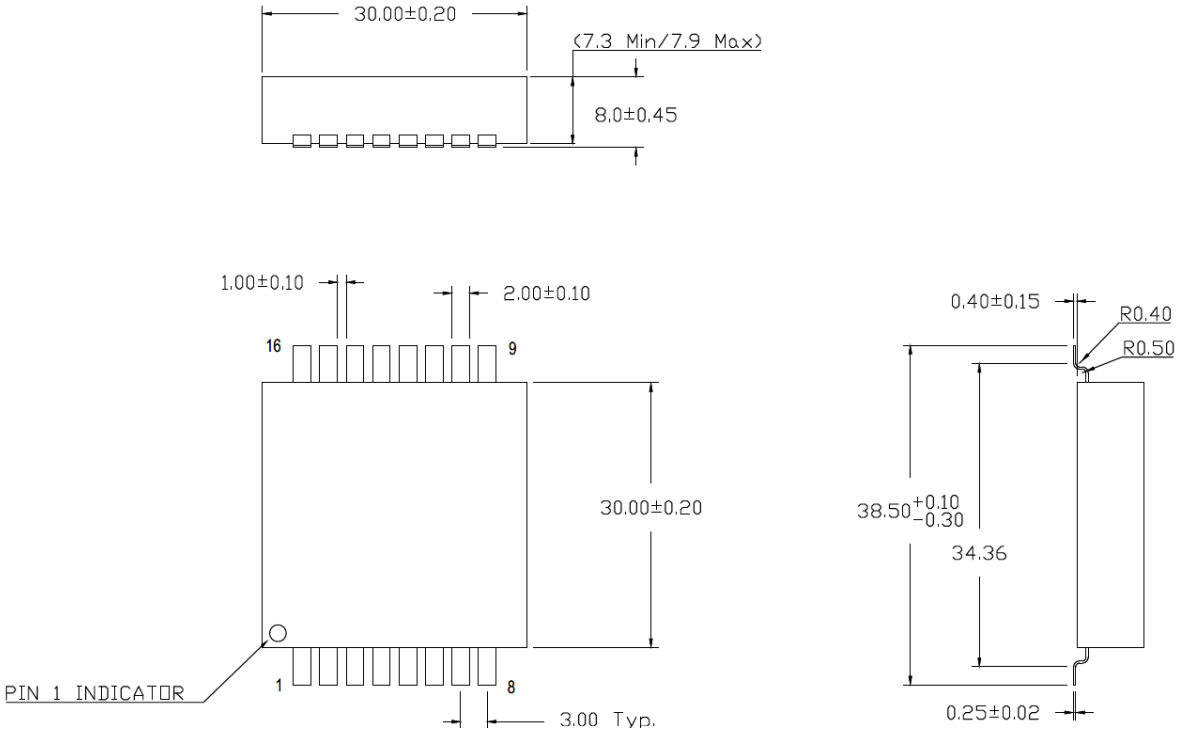


Figure 23 Package Outline

10.2 Marking Information

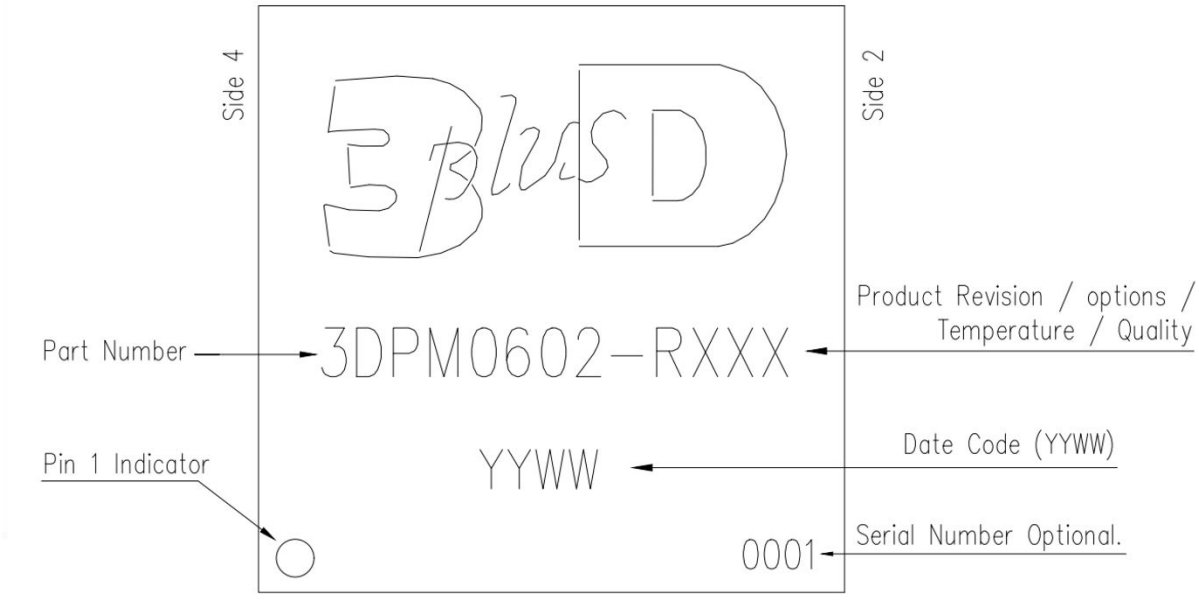


Figure 24 3DPM0602-1 Marking Information

11. Ordering information

Part Number	Temperature Range	Screening Level	Package
3DPM0602-1 IB	-40°C to +85°C	Industrial	SMD package with gull-wing leads (16)
3DPM0602-1 SB	-40°C to +105°C	Industrial	SMD package with gull-wing leads (16)
3DPM0602-1 IS	-40°C to +85°C	Space	SMD package with gull-wing leads (16)
3DPM0602-1 SS	-40°C to +105°C	Space	SMD package with gull-wing leads (16)

Table 10 Ordering Information

12. Contact Information

FRANCE	3D PLUS 408, rue Hélène Boucher ZI. 78532 BUC Cedex	Tel : 33 (0)1 30 83 26 50	**Web :** www.3d-plus.com **e-mail :** sales@3d-plus.com
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Table 11 Contact Information

13. Notice and Disclaimer

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(2) designing, validating, and testing their final system implementation, and
(3) ensuring that their design complies with all applicable safety, reliability, security, and regulatory requirements.

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