VERY HIGH SPEED 3D "SYSTEM IN PACKAGE"

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1. Introduction

Decoupling is a long-standing problem which our first works carried out on VHSIC decoupling, which at that time linked 100 bits, led to significant power noise reductions (réf. 1 and 2).
Recently, WINKEL (ref. 3) made it clear that "*Modern, especially high integrated, systems needs new, the so called hierarchical decoupling strategies, in order to cover the high-mid-and low frequency range. The capacitor type and placement in all packaging levels is essential for the effectiveness of the decoupling strategy*". The same problem occurs when dealing with on-chip power supply integrity during operation (ref 4). It goes without saying that the coming up of 3D interconnection, while reducing the length of the interconnections between the chips, enables to reduce the inductances. However, if we want to keep the integrity of the signal coming from the chips, improvements should be made even at the 3D interconnection level by integrating horizontal and vertical capacitors inside the 3D module.

We present a study carried to analyze the signal integrity and the EMI/EMC aspects of a 3-D module made by stacking four layers of 256 Mbits SD-RAM Small Outline Packages. The additional lead lengths in the vertical stack, and the high dI/dt concentration could create potential problems. Internal EMC aspects (power integrity, Cross-talk) as well as external ones (ground bounce, noise pollution of the host PCB, radiation) are reviewed in this paper, with several drastic solutions.

2. 3D cubes structure

3D PLUS interconnection technology applies to bare dice and plastic packages (CSP, TSOP, etc). TSOPs plastic packages are the most frequently used, being the most available on the market, as well as the cheapest. The versatility of our 3D technology allows to stack different kind of components in order to elaborate memory cubes, computing cubes and microsystem cubes (see figure1). We first worked on the TSOP stacking problem:

- Pick and place of the TSOPs on a lead frame.
- Stacking/gluing of these sets.
- Cutting.
- Plating.
- Laser etching.

A comparison between 3D and 2D has been performed on 256 Mbit SDRAM TSOPs in DIMM bare :

- 8 TSOPs for 2D DIMM.
- 8 modules of 4 TSOPs stacked for 3D DIMM.

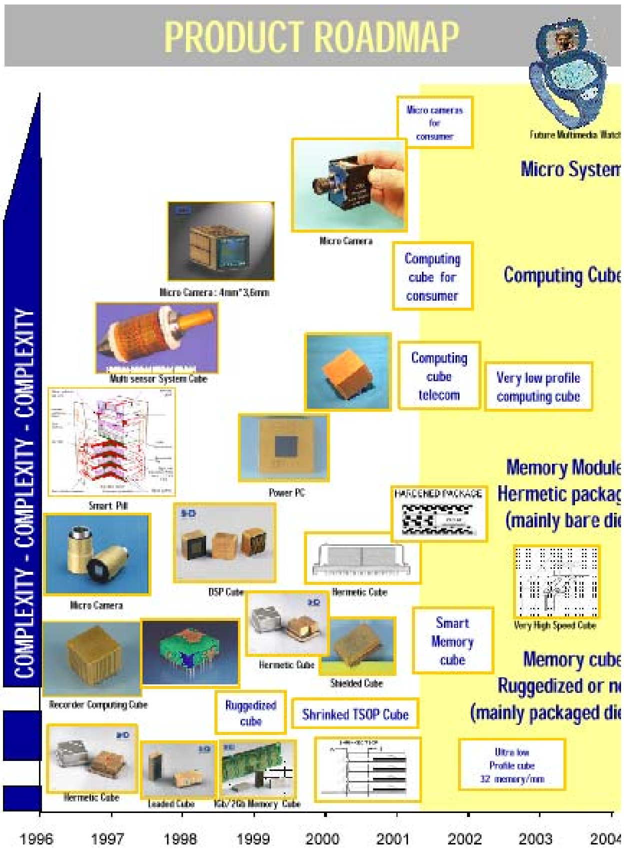

Figure1 : product roadmap

The measurements made on Dan-Elec's DIMM by INFENEON exhibit better results for 3D DIMM (ref. 5):

- Consumption : decrease from 3 to 10%
- DC Level : increase of noise immunity, from 500mV for 2D DIMM to 900mV for 3D DIMM.
- Speed : improvement of 1.8ns (20%).
- Capacitance : decrease of 100%.

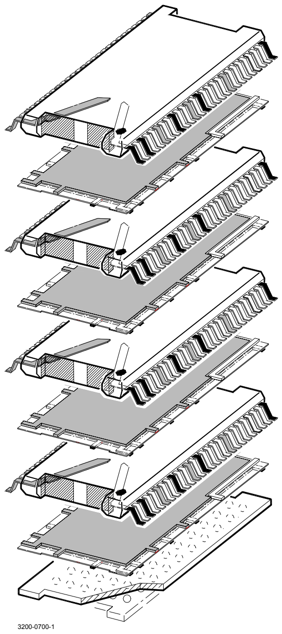

Figure2: Stacking structure of 3DPLUS' memories with vertical and horizontal capacitors

The integration of capacitors within each TSOP as well as the placing of vertical capacitors, i.e. perpendicular to the inter level capacitors, allows both to store energy as close as possible to the chips and to bring additional energy, thanks to the vertical capacitors acting as vertical bus bar. This capacitor placed as close as possible to the demand, named "Embedded Power Integrated in a Cube", is referred to under the acronym EPIC. The stacking structure is presented on figure2.

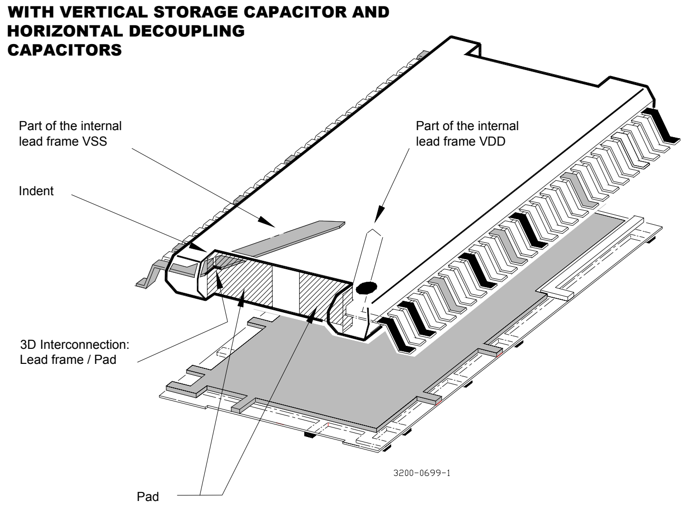

Figure 3: Part of the structure with 3M's capacitor foil

Figure3 shows a part of the stacking with 3M™C-Ply Embedded Capacitor Material, made of a dielectric foil between 2 copper foils of 35 µm each. The total thickness of the capacitor is 75 µm.

It can be observed that all the V_{SS} and V_{DD} are connected to corresponding leads on the capacitor. Moreover, the ground copper plane is used to route the Chip select etc…

Stacking of these capacitors allows shielding the memories. An indent made through a grinding on the whole height of the cube can be seen on the TSOP. This indent allows reaching directly the V_{SS} and V_{DD} leads of the lead frame, thus minimizing the inductance between the vertical capacitor and the lead frames.

Figure4 shows the whole cube, with the 2 vertical capacitors placed in indents.

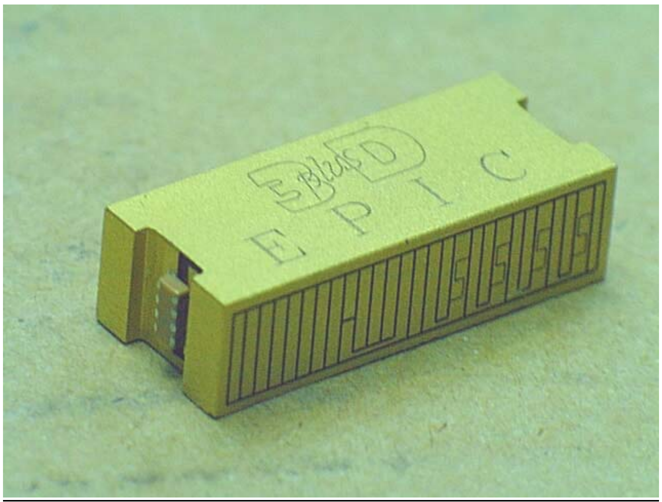

Figure 4: 3DPLUS'memory cube with vertical and horizontal capacitors

3. Signal integrity at the TSOP level

3.1 Transient Noise on DC Voltage and Ground Distribution

The worst, yet realistic scenario is the case where 8 I/O bits are switching simultaneously. The following dynamic parameters are typical of the selected LV-TTL family: where the output voltage slope (10% - 90%) is : 2V / 1ns (see figure5).

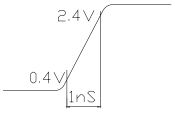

Figure 5: Rising front of the signal

3.1.1 Currents

Three currents must be considered (see figure6):

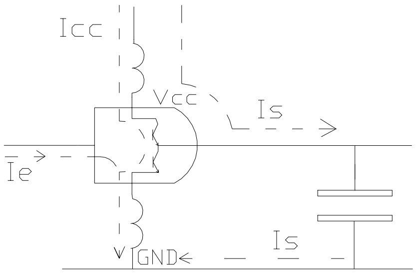

Figure 6: Transistors in a totem-pole arrangement

3.1.1.1 The switch-through current (I_{cc}).

I_{cc}: 10mA/device.

It is caused by the temporary conduction overlap of the two output devices (in a totem-pole arrangement, one of the output transistors is already "on" while the other is not totally "off", yet).

The layout arrangement is quite favorable. A majority of V_{cc} traces are located at 2 or 3 intervals from a Gnd trace. A slight improvement would have resulted by alternating systematically V_{cc} - Gnd - V_{cc} - Gnd etc, but the pattern is imposed by the basic TSOP. There are seven V_{cc} + Gnd pairs, with:

- Mean path length = 4.3 mm
- Linear inductance ≈ 0,8nH / mm

So for one single V_{cc} (or Gnd) trip equivalent inductance:

$$\boxed{L_v = 0.8 \times 4.3 / (7 \text{ traces in } //) = 0.5 \text{ nH}}$$

3.1.1.2 The instantaneous output current (I_s)

It is driven in (or from) the capacitive loads. For a total output load of 20pF (4pF for driven device + 16pF for trace): $I_s = C\,\Delta V / \Delta t = 20.\,10^{-12}.\,2V / 1.10^{-9}$ s

$$\boxed{I_s = 40\text{mA/device.}}$$

The worst situation occurs with a falling front, whereas I_s return by the Gnd traces and pins, while the logic noise immunity is generally lower.

- Worst I/O terminals (the longer ones): # 20-22, 34 – 36.
- Shorter ones, and nearer to a Gnd: # 8,11,16,17 etc
- Mean path length: 4.3mm
- Linear inductance: 0.9 nH/mm (because the average distance to a Gnd is larger)

So for the I_s sink via 7 Gnd traces in parallel, the equivalent inductance is:

$$\boxed{L_g = 0.9 \times 4.3 / (\ 7 \text{ traces in } //\ ) = 0.55 \text{ nH}}$$

3.1.1.3 The additional consumption I_e.

This current is due to the 3 ancillary signals which could be switching at the same time (two Clocks and one Chip Select). It appears that these are not "current hungry", since the TSOP is simply a subscriber for these signals, without drivers. So, for these lines, we consider only the peak current imposed by the input capacitance alone, i.e. ≈ 4pF:

$$I_e = 3 \times 4.10^{-12}.\,2V / 1.10^{-9}$$

$$\boxed{I_e = 24\text{mA}}$$

Notice, however that the TSOP is receiver for these signals, such as the input capacitances are:

- Charging up for a rising front: currents Ie are sunk down the Gnd pad.
- Discharging for a falling front, hence Ie are coming up off the Gnd pad

3.1.2 Voltage drop

Table I shows the individual contribution of I_{cc}, I_s and Ie along the V_{cc} and Gnd paths.

	n x I_{cc}	n x I_s	I_e	Σ I
Rising front				
for V_{cc} pin / pad	↓	↓	0	$I_{cc} + I_s$
for Gnd pin / pad	↓	0	↓	$I_{cc} + I_e$
Falling front				
for V_{cc} pin / pad	↓	0	0	I_{cc}
for Gnd pin / pad	↓	↓	↑	$I_{cc} + I_s$ - Ie

Table I. Respective Directions of I_{cc}, I_s and Ie during positive and negative transitions.

We see that the input currents Ie are minor contributors during a rising front, and actionless, or subtractive during a falling front. Therefore, we can build our estimate of switching noise based on the sole I_{cc} (x n bits) and I_s (x n bits).

- Voltage drop along the V_{cc} pad-to-chip path (rising front)

$$\Sigma\, L_v\, dI/dt = 8 \times (0.5\text{nH} \times (10\text{mA} + 40\text{mA})) / (1.10^{-9}\text{s})$$

$$\boxed{\Sigma\, L_v\, dI/dt = 0.2\text{V}}$$

- Voltage drop along the chip-to-Gnd pad path (falling front)

$$\Sigma \cdot L_g\, dI/dt = 8 \times (0.5\text{nH} \times 10\text{mA} + 0.55\text{nH} \times 40\text{mA}) / (1.10^{-9}\text{s})$$

$$\boxed{\Sigma \cdot L_g\, dI/dt \approx 0.2\text{V}}$$

These values, caused by the TSOP alone, are representing about 50% of the worst-case DC noise margin for the LV-TTL family, and about 25-30% of the AC noise margin for a 1ns pulsewidth. We may say that this noise is intrinseque to this off-the shelf 54-pin package.

3.2 Capacitive Cross-talk

Although both capacitive and magnetic cross-talks do take place, the capacitive is the dominant one, due to the rather low currents, compared to the significant values of dV/dt applied to the trace-to-trace mutual capacitances, enhanced by the dielectric constant in the package.

For the following worst case configuration:

a) Culprit and victim trace are very close (one interval)
b) Culprit and victim traces are far from a Gnd trace (6 intervals for pads like #20,34,35)
c) One culprit line is active with 2V/1ns
d) Victim trace is next (average spacing 0.32mm on TSOP, 0.5mm on vertical runs)
e) Victim trace, at LOW state is seen as a high Z on TSOP near end; ex: 1MΩ // 4pF
f) Depending how far is its other end; the output resistance of the source or the characteristic impedance of the line also loads the victim line (on the host PCB).

The total coupling capacitance seen by one level is: $C_{1\text{-}2}$ = 0.32pF (see the equivalent circuit in figure7).

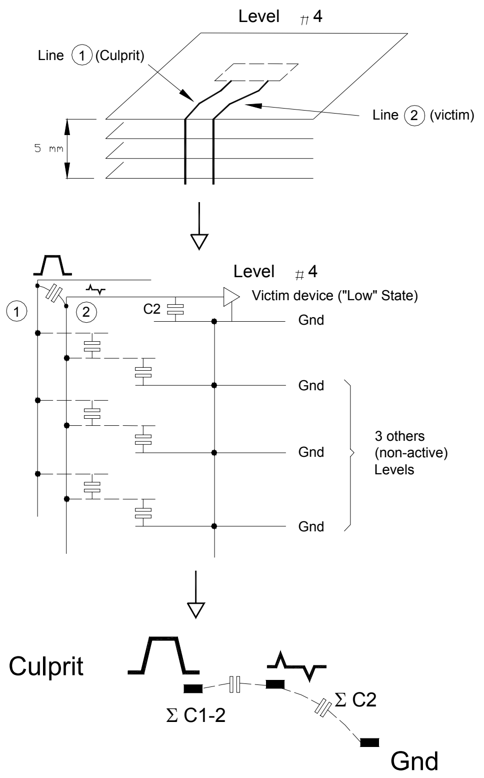

Figure 7: Equivalent circuit for cross-talk (capacitive)

The total victim impedance (source and load in //), for a 1ns rise time is: $Z_v \approx 60\Omega$.

4 Signal integrity of the 3D cube.

This memory module is a 2 banks x 512Mbit x16 Synchronous DRAM composed of four 8 bits 256 M-SDRAM TSOPs stacked. The first bank is composed of TSOP 1 and 3 and the second one of TSOP 2 and 4.

4.1 V_{cc} & Ground Bounce

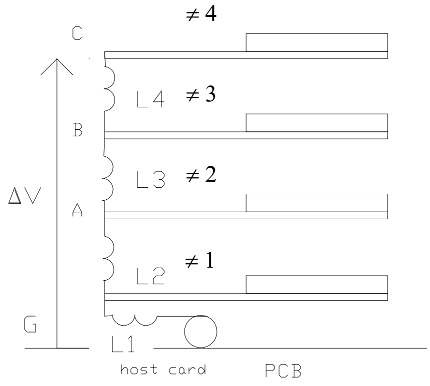

Figure 8: Equivalent circuit of the 4-level stack

Since we are dealing with a ball grid array (BGA)(see the equivalent circuit given in figure8), the self-inductance between the #1 level and the ground plane of the host PCB is very small, estimated as:

$$L_1 \leq 0.2 \text{ nH (for one line)}$$

For the 7 vertical drops along the sides, their width (0.4mm)/length (1.2mm) ratio is large, giving a rather low value of linear inductance:

$$L_2 = L_3 = L_4 = 0.4\text{nH /mm x } 1.2 \text{ mm} \approx 0.5\text{nH}$$

During simultaneous switching, the worst situation for our 4-layer stack occurs when 8 bits are changing in levels #2 and #4. The associated vertical voltage drops, from each level to ground are:

a) Level #2 vs. ground

$\Delta V_{A-G} = Lx\ (dI_{(2)}/dt + dI_{(4)}/dt)$
with L= [(0.5nH + 0.2nH] / 7= 0.10nH
$\Delta V_{A-G} = 0.08V$

b) Level #4 vs. ground

$\Delta V_{C-G} = \Delta V_{A-G} + L\ dI_4/dt$
with L= [(0.5nH + 0.5nH] / 7 = 0.14nH
$\Delta V_{C-G} = 0.14V$

Summing TSOP voltage drop and vertical package voltage drops, we get the total ground shift seen from level#4, during an 8-bit simultaneous switching at levels #2 and #4:

ΔV (chip#4 to Gnd) = 0.2V (TSOP) + 0.14V (cube)

ΔV (chip#4 to Gnd) = 0.34V

This is still below the worst-case static noise margin, and represents ≈ 60% of the AC noise margin for a 1ns pulse.

4.2 Cross talk

4.2.1 Contribution of vertical drops and other levels

At the cube level, each vertical run sees also, in parallel:
- the stubs of horizontal traces to the 3 other, non-addressed levels, with their own contribution to the trace-to-trace capacitance (this increasing the total C_{1-2} value)
- the input capacitances of the other, non addressed inputs (this reduces cross-talk)

4.2.2 Total Cross talk

Taking into account all the above parameters, we reach total values of:
$C_{1-2} = 1.1\text{pF}$ and C_2 (victim capacitance to Gnd) = 16pF
Actual cross talk: 120mV
Worst possible cross talk (asymptotic value) = $C_{1-2} / (C1_{-2} + C_2) = 0.065$, or -24dB
These values will grant a low risk of self-jamming

4.3 Comparison with criteria for self-jamming and external EMI

4.3.1 In terms of functionality:

The 3-D package is still below the self-jamming threshold for LV-TTL. However, in the worst-case configuration of simultaneous switching, more than half of the noise margin is eaten-up by the V_{cc} & Gnd distribution noise, even if a perfect decoupling capacitor is installed at the package footprint. This will oblige the designer of the host PCB to take significant precautions at the board level, like multilayer board, careful layout of the critical traces etc.

4.3.2 In terms of the EMI generated by the host equipment:

The whole TSOP signal reference (V_{ss}) is fluctuating with this ground noise, at the clock frequency or any frequency of the synchronous transitions. This Common Mode HF noise is polluting all the I/O lines, even the low speed or steady lines. This will "export" CM noise towards the equipment I/O connectors, ribbon cables and external cables, aggravating the EMI radiation of the entire machine.

5 Improvement with horizontal planar capacitors

By installing a dedicated planar capacitor (3M™C-Ply Embedded Capacitor Material) under each layer, the following improvements result, compared to the bare 4-level module (see figures 2 and 3). Therefore, the hierarchical decoupling strategy consists in placing the energy supplier as close as possible to the component, in order to minimize the inductance.

5.1 Instantaneous power storage

The capacitor value has been conservatively estimated as 5nF per TSOP (≈15nF/sq.in.). With such value, the peak current demand for one TSOP in our worst-case scenario of 8-bit simultaneous switching, can be provided by this local reservoir, with a source voltage drop approximated by:

$$\Delta V = \Delta I.\Delta t/C$$

Where $\Delta I = \Sigma$ switch-thru currents I_{cc} + instantaneous currents Is (see par. 3.1) = 8 x 50mA / TSOP.

$$\Delta V = 0.4 \times 10^{-9} / 5.10^{-9} = 0.08V$$

Notice that this voltage drop is combining with the 0.2V inductive drop, intrinseque to the device, along the TSOP leads (calculated in par.3.2).

Total "voltage starving" at chip level: 0.28V

We assume that the flat capacitor armatures underneath the TSOP do not reduce the value of V_{cc} and Gnd lead inductances. More exactly, we considered that this self-inductance, related to the flux interception in the loop area, does not change for the V_{cc}-Gnd paths in the horizontal plane (leads on the same side). It would change for loop areas in the vertical plane, i.e. for those V_{cc}-Gnd pairs on opposite sides of the package. However the capacitor armatures cannot be regarded as a perfect, infinite plane, but an edge-limited stripe. Therefore, to be on a conservative side, the self-inductance values have been kept the same as for the bare TSOP. If the capacitance value could be increased to 8-10nF, the voltage drop at capacitor output would be only 50-40mV, thus improving its overall efficiency.

5.2 Decrease of the vertical voltage drops

Without any capacitor in the 3-D package, a significant share (45%) of the power distribution transient noise is caused by the peak current demand through the inductance of the vertical V_{cc} /Gnd distribution busses (see par. 4.1). These inductances are still there, but the large dI/dt are now delivered by the local capacitive storage, such as less LdI/dt voltage drop is affecting the power supply.

5.3 Cross-talk reduction

The capacitor ground armature acts as an electrostatic screen against the lead-to-lead cross talk between two levels of TSOP. Although this cross-talk contribution is rather weak (typically ≤50mV), this decrease improves the overall EMC margin within a 3-D module (see figure9).

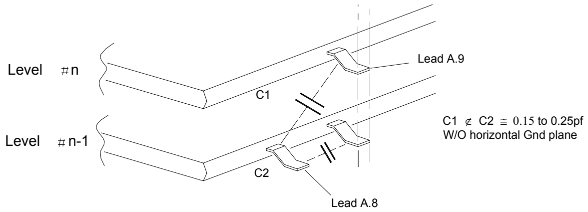

Figure 9: Equivalent circuit

5.4 Equipotentiality

By interconnecting all the Gnd leads (or V_{cc}) at a same level, the capacitor armature tend to equalize the voltage difference between a given layer and the host PCB reference.

5.5 What the horizontal capacitors will not do

The vertical bus inductances still remain in series in the signal path between a given TSOP and its external interface (see figure10). For instance, during 8 simultaneous falling fronts, the 8 currents "sink" are crossing the vertical Gnd bus impedance, causing a series voltage drop Δ_{VB-C} which is cutting into the functional noise margin in a module-to-module dialog.

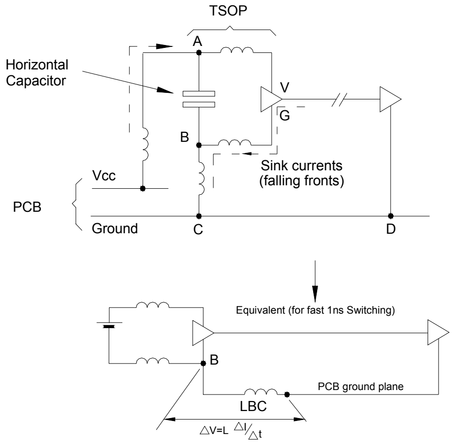

Figure 10: With the horizontal capacitor, the signal current return path is still affected by the 3D cube vertical inductances.

This voltage shift (80-100mV) has been calculated for the bare 3D-module, and is not reduced by the horizontal capacitor.

6 Improvement brought by vertical, multilayer leadless capacitor banks (see figure11)

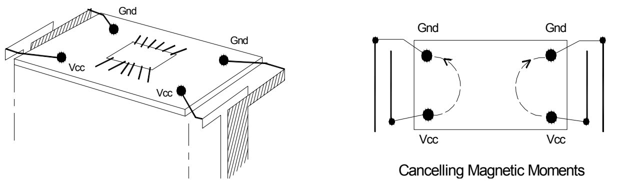

Figure 11: Equivalent circuit for 4-level package with two side capacitors

We are looking here at the benefit brought by vertical, leadless capacitors located at the small sides of the module, exclusive of the horizontal capacitors discussed in 5.

The transitional switching current (pulse width ≈ 1ns) is partly supplied:

- From the vertical AVX capacitor, with its associated low distribution inductance (estim. $L_{gnd} \leq 0.5$ nH).
- From the host PCB power distribution, via the 7 vertical power busses (V_{cc} or Gnd).

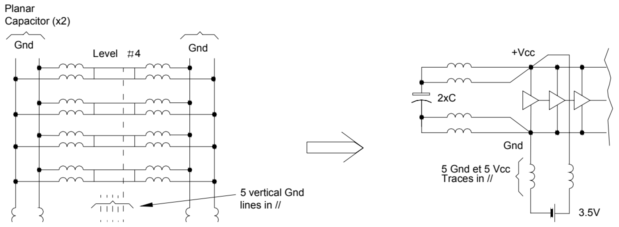

Figure 12: Simplified equivalent, for one (any) level

We can calculate the size of the ideal capacitor (see the equivalent circuit in figure12), if it was to feed the total current demand during our worst case scenario of 2 x 8-bit simultaneous switching:

$\Sigma I\Delta t = C . \Delta V$ With $\Sigma I = 2 \times 8 \times (10 + 40\text{mA})$ and $\Delta t \approx 1$ns

ΔV is a deterministic parameter, given the allowable voltage drop that the designer decides he could afford. If we allocate a very conservative value of ≤ 10% of the noise margin to the V_{cc} and Gnd distribution noise, we get:

$$C = 0.8A. 1.10\text{-}9 \text{ s} / (0.1 \times 0.4V) = 20nF$$

Eventually, this capacitor will also provide some of the TSOP demand during a memory refresh cycle. With these values of capacitor, residual inductance and instantaneous current demand, the total calculated ground bounce for worst case conditions will drop to 0.28V.The major benefits of this arrangements are:

a) The reservoir capacitor is now very close to its points of delivery.

b) Some of the vertical voltage drop along the V_{cc} and Gnd busses is eliminated.

c) The Common Mode Ground bounce of all the V_{ss} (and especially level #3 and 4) versus the host PCB ground reference is eliminated.

7. Overview of the total improvement with horizontal /vertical capacitors (see figure13)

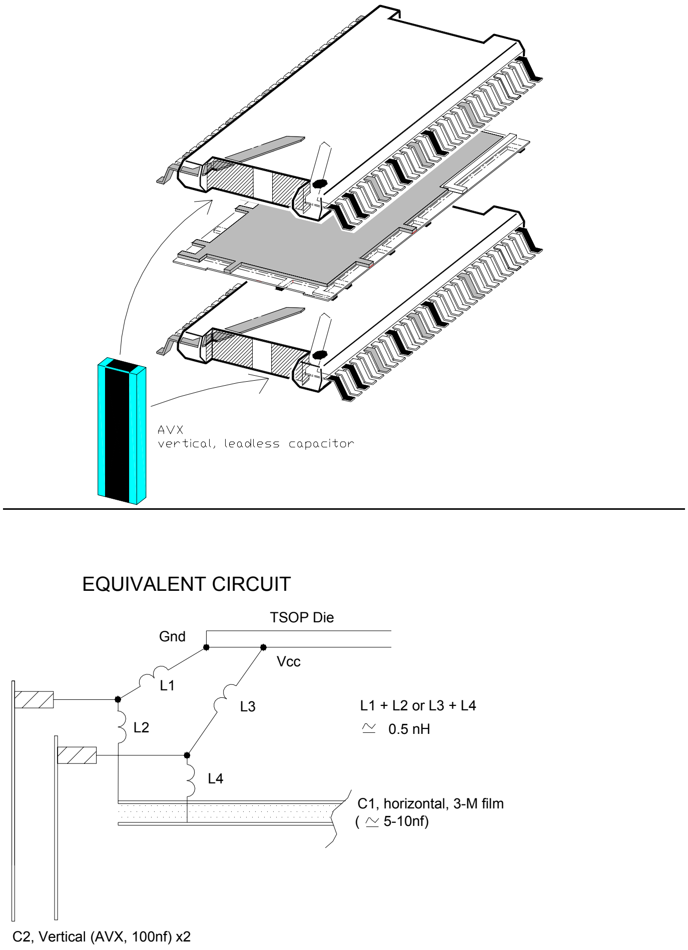

Figure 13: Combined effects, horizontal and vertical capacitors

The combination of horizontal and vertical leadless capacitors is adding the respective benefits of both solutions (par. 5 and 6). By creating a 3-D criss-crossing of low-impedance V_{cc} and Gnd strips, with embedded capacitances in between, both the internal EMC (no self-jamming) and external EMC (less transient noise and ground-bounce) are improved.

Notice that the vertical capacitor armatures are branching, through wide metallizations, to a mid-point of the V_{cc} and Gnd leads such as the vertical capacitor is acting both:

a) as a partial storage for the TSOP instant current demand (the portion that the horizontal cap does not deliver)
b) As an intermediate "bucket-brigade" element for re-charging the horizontal capacitors from the PCB main supply source.

8. Radiated Emissions of the 3-D Module alone

The radiated emissions of the 3-D package have been calculated, using the simplified method of the maximum electromagnetic moments, applied to a "reasonable" worst case scenario (ref. 6):

a) discrete spectrum: one 125MHz clock signal permanently delivered to the 4 levels

b) random spectrum: 16 simultaneous switching (8 bits on level 4, 8 bits on level 3)

We have neglected, after a coarse evaluation, the contribution of the V_{cc} capacitors discharge loops. Since the two capacitors are facing each other, their magnetic moments are ≈ cancelled.

8.1 Narrowband (clocks) and Broadband (NRZ signals) source spectra

The following respective voltage and currents waveforms have been used for calculating each spectrum.
For the Narrowband spectrum, each harmonic is seen as a discrete frequency term whose amplitude is calculated in Volts.

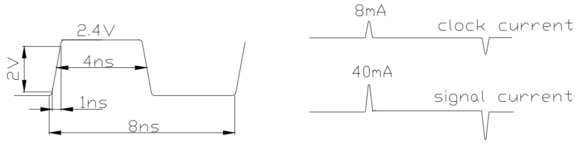

Figure 14 : Clock and signal current

The peak clock current is ≈ 8mA (see figure14). For the Broadband spectrum, there are no discrete harmonics, and it is expressed by its spectral density, in Volt / MHz. The peak current is defined by the 20pF capacitive loading of the outputs, i.e. Is = 40mA / line. The switch-thru current I_{cc} (see par. 2) is discounted, since all the 16 magnetic moments will more or less neutralize each other, considering their current paths from and to the vertical decoupling capacitors.

8.2 Geometry of radiating loops (horizontal and vertical)

(see figure15)

The following geometries have been used for the clock distribution and address/data. Since the clock is distributed over the 4 levels, an average surface (36 mm2) has been entered. For the random data, the average radiating loop is larger, since the next ground return trace is typically farther away. For the average loop (mean dimensions for levels #3 and 4), each loop area is 15 mm2, so a total of 240 mm2 for the 2 x 8 loops.

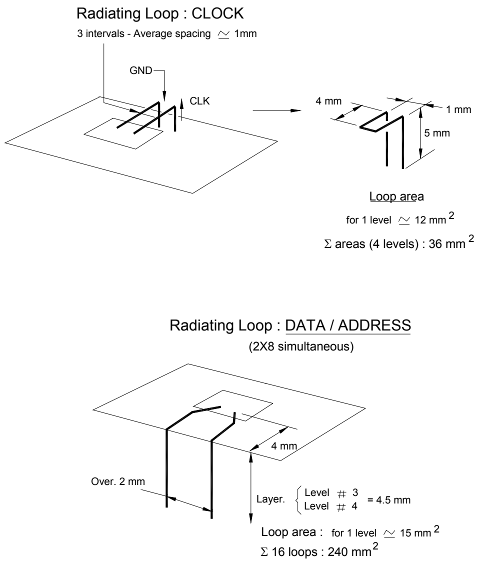

Figure 15: radiating loops estimate

8.3 Radiated Field @ 1m for worst case 4-chip activity

We have made an estimation of the radiated field at a 1m distance, in the standard 120kHz receiver bandwidth, due to the 3-D module alone, without any shielding effect at the board or the host machine .The contribution of the host PCB and external cables would be typically much higher, until some suppression techniques are applied at the packaging level.
As predictable, the radiated spectrum is dominated by the Narrowband contents, although some Broadband emissions are not very far below. It is interesting to see that the module-alone radiation is way below (20 - 22dB) the most severe radiated limit of Civilian class B (US-FCC or European CISPR 22) limit. It even meets, without any shielding, the most severe category (Aircraft equipment) of the Mil Std 461 RE02 limit.

9. Conclusions

The 3-D Plus package with four TSOPs, especially with the integrated vertical and horizontal capacitors, stays well inside the acceptable noise margin of the LV-TTL family. In particular, the embedded capacitors underneath each layer provide a power distribution quality that could not be reached with a traditional PCB-mounted supply capacitor. The RF field radiated by the module alone, based on a 125MHz clock and maximum chips activity, is 20-22 dB below the FCC and CISPR class B limits, and can even comply with the severe Mil 461-RE02 limit for airborne equipment.
The simulation shows that the hierarchical decoupling strategy is very efficient. Nevertheless, it suffers from the parasites induced by the TSOP itself: We could see that the TSOP can represent up to 50 % of the DC noise margin of the LV-TTL family and about 25/30 % of the AC noise margin of 1 ns Pulse Width.

This is why we developed what we call the Srunk TSOP, which consists in stacking the TSOPs exactly as described, and saw them not outside (A) each TSOP but inside it (B) (see figure16). This leads to cubes, whose sizes, depending on the size of the chip, are equal to those of the Chip Scale package.

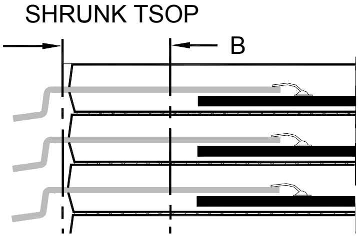

Figure 16: TSOPs shrinked

We have not made any simulations yet or tested the integrated decoupling on this type of products. This will be done during the first semester 2001.

3D Plus also stacks CSPs, using this strategy (see Figure17).
The plating used for 3D technology enables to get very low resistance from the capacitors, thanks to the use of a thick copper.

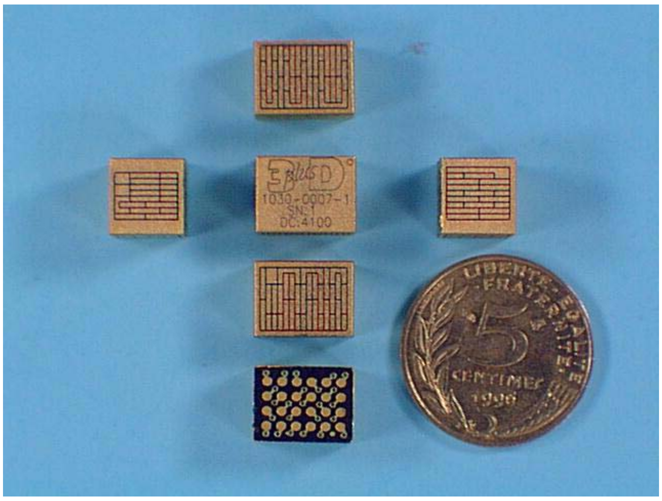

Figure 17: Memory modules composed by CSPs stacked

The application of this concept (EPIC) is made on stacked memories (SDRAM, SRAM and DDRAM). It is being used for stacked DSPs and FPGA. Of course, it can be applied to 3 dimension System In Package “SIP”.

10. References

1- C. VAL, J. MARTIN “A new chip carrier for high performance applications: integrated decoupling capacitor chip carrier”. Proceedings of the 2nd International Electronics Packaging Society Conference, San Diego Nov 15-17, 1983.

2- C. VAL. “High performance electrical and environmental surface mounting VHSIC packages”. Proceedings of the 4th International Microelectronics Conference May 28-30, 1986, Kobe, pp 98-107

3- T.M. WINKEL. ”Decoupling strategy and decap hierarchy structures”. The 2001 European Systems Packaging Workshop. January 22-24 2001, Barcelona.

4- R. FRECH Personal communication

5- .J. MARQUET, Dan-Elec, Personal communication

6- M. MARDIGUIAN Controlling Radiated Emissions by Design – Kluwer Academic Press, Boston.