

High-Density Packaging for Spaceborne Electronics

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Introduction

It is well known that spacecraft electronics have requirements that far exceed electronics for military, avionics or commercial applications. These additional requirements include some measure of total dose resistance to the protons or electrons trapped in the Earth's magnetic field, as well as immunity to single-event induced latch-up. Of course the actual radiation tolerance requirements can be extreme, depending on mission, with additional specifications for single event upset, neutron fluence and prompt dose survivability. In addition to the radiation requirements, spaceborne electronics almost always have very stringent reliability requirements (since the vast majority of spaceborne electronics are non-repairable) with failure-rate specifications of less than 10 failures/billion-device hours being a common requirement.

Of course, regardless of how stringent the requirements for satellite electronics, the reality is that the system must be capable of performing its mission. This "push-pull" between mission performance and mission assurance is probably at its greatest in spaceborne electronics. As noted above, space presents a truly unique environment and thus unique challenges to the mission assurance teams. However, just because the spacecraft may be stationed in a tough environment, doesn't allow the systems designers the luxury of easing off on mission performance.

One of the greatest challenges for spacecraft electronics designers is to meet mission requirements using radiation-hardened electronics that are frequently several generations behind commercial components in terms of performance, density, etc. Because of this "generation" gap more and more commercial components (COTS) and technology (COTS) are finding their way into satellite electronics. One such technology is high-density stacking. The spacecraft industry can reap large benefits from stacking technology. Satellite launch costs can run up to U.S. \$10,000/pound with very strict limitations on the total PC board area. Stacking devices can dramatically reduce both weight and area. Of course, stacked devices must meet the same strict requirements for radiation tolerance and reliability as traditional monolithic or multi-chip module (MCM) solutions. That's been the challenge, finding a commercial stacking technology that can survive the rigors of "Class S" type screening.

High-Density Stacking for High-Reliability Applications

Stacking ICs to improve density is certainly not a new idea. Stacking has been around for a number of years. Most of the current stacking technologies are well suited to the commercial electronics market, i.e. it's reliable enough and it's very inexpensive. Unfortunately, these commercial stacking technologies can not meet the

rigorous requirements for most satellite electronic applications. However, a new stacking technology developed at Thomson-CSF and brought to production by 3D Plus Electronics has recently passed a full QML V / Class S- type qualification. The parts were delivered and approved by NASA for a LEO observation mission. The novel stacking approach starts with either bare die or packaged devices (packaged device types most commonly used are TSOPs). The stacking technique comprise five primary steps :

- Stacking/molding with low-outgassing epoxy (Dexter Hysol)
- Cutting with dicing machines
- Plating with Ni Ni/Au
- Patterning etching
- Final electrical test

The real elegance of this approach is that it uses very few steps with relatively inexpensive raw materials while producing a device of exceptional ruggedness.

Figure 1 shows the basic flow for the stacking process. There are a few important points to note: 1) The process is straightforward yielding a final product that is indeed very rugged (essentially a solid epoxy cube), 2) There is no solder used in the process, all the electrical routing is done by the Ni/Au outer layer, which removes the single largest reliability and quality concern of stacking, and 3) The sawing process after molding can cut into the existing TSOP package so that the final cube can have a smaller area than the original monolithic TSOP.

Stacking for Spaceborne Electronics

So far we have discussed stacking primarily from a mechanical standpoint, i.e., assembly flow and structural rigidity. As we have shown, the rugged stacking approach is an ideal candidate for spaceborne applications from a mechanical standpoint. It has a much smaller footprint than an equivalent ceramic/hermetic multi-chip module (MCM), and has significantly less mass. Unlike more commercially targeted stacking approaches, the rugged stack described here can easily survive the stringent QML V Group D qualification testing of thermal cycles, thermal shock and shake and vibration testing.

However, mechanical or structural integrity is obviously not sufficient to ensure a successful mission in a spacecraft. Before electronic devices can be used in spaceborne applications, the electrical reliability and radiation hardness assurance must also be guaranteed. In this section of the paper we will focus on radiation and reliability issues associated with using stack technology in space. In general, stacks do not affect the reliability or radiation performance significantly (either positive or negative). The individual ICs in the stack may operate at a somewhat higher temperature compared to an equivalent MCM device; however, when normalized for temperature, the radiation response and reliability are essentially identical.

Stacking components does offer several advantages over MCMs (in addition to the area and weight savings). The single most important advantage is a significant reduction in yield loss for "Class S" type components. Class S components that use a silver-glass die attach technique can not be reworked. So a single bad die in the MCM will cause the scrapping of the MCM. Although the die are probed at wafer level (usually at room temperature only) we find that individual failure rates of about 10-15% occur following burn-in and three temperature testing. This is particularly true for many SRAMs, which show the highest percentage of fall-out at low temperature testing. A 10% fall-out rate on individual die within an MCM leads to a reduction in yield by 0.9 to the 4th power. That is, the yield of the MCM will be 66% if each individual die yields 90%. If each individual die yields only 85%, then the MCM yield plummets to just 52%.

Of course a known good die program could be instituted to improve the MCM yields. Known good die tooling consists of a custom-tooled die carrier and socket. This approach does indeed dramatically improve the MCM

yield; however, the tooling costs are very high, the cost to handle the parts rises dramatically and there is usually a large loss of die due to mishandling during insertion into the die carriers (usually scratching). In all but extreme cases, known good die programs are generally not employed because of the expense and handling difficulties.

Conversely, stacking utilizes parts that are “packaged” either in TSOPs or on flex tape. This greatly facilitates handling during test and burn-in with no expensive tooling costs. The individual components to be stacked, whether in TSOP type packages or on flex-tape, can be easily tested and burned-in prior to stacking. This dramatically improves stack yield (our experience is that it is very close to 100%) and ultimately, a reduced cost to the customer. Figure 2 highlights the difference between a stack flow and an MCM flow.

Radiation Hardness Assurance Using Stack Technology

Integrated circuits used in spaceborne applications need to have some level of radiation hardness assurance. In general, components need to be qualified and assured for total ionizing dose, single event latch-up and single event upset. As mentioned above, the stacking procedure itself does not significantly affect the radiation performance. There are some (usually) minor differences. The stack contains less heavy metals and may reduce the dose enhancement effect for certain space environments. There may be differences in the total amount of shielding in the stack that may reduce the total electron dose slightly (particularly for the center die). But in general, there are no significant differences between the radiation hardness of a stack or an MCM. Ultimately, the final hardness of the stack or MCM will be determined by the hardness of the individual components.

There are three primary advantages of stacking versus traditional MCMs in spaceborne applications: 1) Area savings, 2) Weight savings, and 3) Providing a higher-density solution for components that could not be manufactured into traditional MCMs. The area and weight savings are obvious and there is no reason to discuss it here. The third advantage is not readily obvious and needs a little discussion.

It is well known within the radiation effects community that many commercial components have the potential to meet certain space mission requirements, particularly LEO type missions of short duration. Many of these components are tested on a wafer-lot by wafer-lot basis and lots that meet certain mission requirements are used to build radiation hardness assured product. Unfortunately, these commercial components are not usually available in wafer or die form, but only as commercially packaged TSOPs (or other similar commercial packages).

Commercially packaged parts are not particularly suited to traditional MCMs, so systems that could utilize radiation-tolerant COTS components may not have had access to a higher-density solution. The ruggedized stack discussed here provides an excellent solution to the problem of using COTS parts with intrinsic radiation tolerance in spacecraft requiring high-density solutions.

Summary

A novel, commercial stacking technology has been developed which uses a minimum number of steps and low-cost starting materials (to be competitive in the commercial marketplace). Recent qualification work for a NASA LEO spacecraft has shown that this technology can be used to produce highly reliable “Class S” type electronics for spaceborne applications. The cube molding process and Ni/Au routing technique combine to produce a lightweight device which can save a significant amount of real estate on PC cards.

The stacking process described in this paper also offers the opportunity to install a low-cost “known good die” program and dramatically reduce the amount of wasted product compared to traditional MCM techniques. The stacking process does not diminish the radiation response of radiation-tolerant or radiation-hardened devices so this stacking procedure can be used with radiation-hardened assured components.