3D System-in-Package: Technology Improvements for Volume Manufacturing

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SUMMARY

• 3D Interconnection Techniques - Overview

• The VIGOR Project and its Objectives

• Design & Technology Developments

• Applications

• Conclusions
3D INTERCONNECTION TECHNIQUES - OVERVIEW

- **Packaged Die**
  - Stacked Packages
    - Same or similar ICs, bus connected
  - Folded Circuit
    - Mixed components & formats, multi-chip, multi-level

- **Bare Die**
  - Stacked Circuits
    - Mixed components & formats, multi-chip, multi-level, very rugged
  - Stacked Die
    - Die designed to stack, very rugged (moulded) but not fully versatile
THE VIGOR PROJECT AND ITS OBJECTIVES

VIGOR : Vertical InteGration of Optoelectronic and Radio (sub)systems

- A collaborative project supported by the CEC through the Information Society Technologies (IST) part of the Fifth Framework Programme

- Objectives :
  - Develop module technology combining the advantages of System-In-Package (SIP) integration with vertical integration.
  - Develop robust and versatile stacking & interconnection techniques, able to incorporate many types of active and passive component and to integrate various functions, particularly opto-electronic and wireless
  - Optimise / industrialise the technology for manufacture at reduced cost and in enlarged quantities
  - Illustrate the improvements in modules having optical or wireless connectivity

- The activities included Test Vehicles for technology development and Validation Prototypes incorporating the developed technologies
THE VIGOR PARTNERS AND THEIR ROLES

**SOLECTRON (Co-ordinator)**
- Project Management
- Assembly Technology Development & Overall DfM
- Assembly of Boards for Modules
- Thermal Characterisation
- Techno-economic Analyses

**3D Plus**
- Technology Development
- Fabrication of 3D Stack Modules

**IXL (Bordeaux Univ)**
- Analyses and Characterisations
- Modelling / Simulation

**BAE SYSTEMS**
- Opto-electronics Technology Development & Integration
- Specification, Design & Build of Opto-Electronic 3D SiP

**Centro Ricerche Fiat**
- Wireless Technology Development & Integration
- Specification, Design & Build of Bluetooth™ 3D SiP
DESIGN & TECHNOLOGY DEVELOPMENTS

- Overview of the 3D SiP Stack Fabrication Process
IMPROVEMENT OF 3D STACK PROCESSES

• Circuit Boards for 3D Stacks
  - Cost reduction
  - Multi-sourceable
  - Selection of dielectric material
    - Avoid leakage paths between tracks at sidewalls
    - Processes compatible with multiple suppliers

• Cube Moulding Compound / Encapsulant
  - Performance, cost and process compatibility, multiple sources

• Sidewall Interconnections
  - Metallisation techniques, wet or dry
  - Laser ablation for patterning
Circuit Boards for 3D Stacks

- The circuit boards are larger than the final cubes, the tracks are cut at the edges of the cubes, to provide connections between the boards.

- Dielectric exposed at the edges of the cubes can provide a potential leakage path:
  - The initial process was to remove all dielectric where the cube edges will be cut, to leave so-called ‘flying leads’.
  - Alternatively, oblong holes can be cut, by laser or mechanically, as dielectric under each track cannot leak current to its neighbours (minimum pitch 0.5 mm).
  - Some dielectrics provide less risk of leakage current, so do not need holes.

Diagram:
- Final size of cube
- Flying leads
- Oblong holes
- No holes

Lower Cost
Generic Test Vehicles

- **Characteristics**
  - 5 Circuit boards (Levels), with packaged & bare-die, passives, daisy chains & BGA base
  - Dimensions: 35 x 35 x 22 mm
  - Weight ~43 gm
  - Sn10 Pb90 balls = 624

- **Fabricated with different materials**
  - Circuit boards
    - S1 – epoxy / aramid
    - S2 – BT-epoxy / glass
  - Moulding compounds
    - M1 – initial, qualified compound
    - M2 – similar product, lower cost
    - M3 – lower modulus, higher CTE

<table>
<thead>
<tr>
<th></th>
<th>CTE</th>
<th>Youngs’ Modulus</th>
<th>Poisson’s Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(x/z)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1</td>
<td>11/110</td>
<td>14.5</td>
<td>0.49</td>
</tr>
<tr>
<td>S2</td>
<td>12/55</td>
<td>30</td>
<td>0.15</td>
</tr>
<tr>
<td>M1</td>
<td>22</td>
<td>12</td>
<td>0.26</td>
</tr>
<tr>
<td>M2</td>
<td>19</td>
<td>11.5</td>
<td>0.26</td>
</tr>
<tr>
<td>M3</td>
<td>32</td>
<td>6</td>
<td>0.26</td>
</tr>
</tbody>
</table>
Environmental Testing & Results

• Thermal Cycling, after 1500 cycles
  - No failures of components or of sidewall interconnections
  - All modules passed except those with mould compound M3 and the combination of BT-epoxy/glass and mould compound M2

• Humidity
  - All modules passed at least JEDEC 3 (40 hrs, 60 C / 60% RH)
  - Modules with M2 passed JEDEC 2a (120 hrs, 60 C / 60% RH)
  - Modules with M3 failed due to delamination during JEDEC 2 (168 hrs, 85 C / 60% RH)
  - Modules made with BT-epoxy/glass and M1 passed JEDEC 2
Sidewall Interconnections

- Replacement of a ‘wet’ process by a ‘dry’ process, to reduce cost

- The initial process used traditional ‘wet’ plating:
  - Electroless nickel / electrolytic nickel / electrolytic gold

- A ‘dry’ PVD process has been developed to replace it:
  - Chromium / copper / chromium

- The equipment was modified to achieve:
  - Deposition of low resistivity copper, 3.3 $\mu\Omega$.cm (bulk copper 1.7)
  - Improved adhesion and reproducibility
  - Process temperature < 140°C

- Ageing tests revealed no differences between the plated & PVD layers

- Interconnections between the Circuit boards are defined by laser ablation
  - Effective on both types of metallisation
OPTO-ELECTRONIC SUB-ASSEMBLY TECHNOLOGY

• Optical Waveguide Splitter / Combiner
  Ÿ Low-loss polymer optical waveguide
  4 : 1 splitter / combiner (3 x 2-way)

• Optical connector
  Ÿ To avoid a fibre-tail, to ease handling & assembly
  Ÿ Modified to reduce size & weight

• Optical, electronic & mechanical co-design
  Ÿ Use of bare-die, to reduce size & weight of
    splitter / combiner and entire sub-assembly
  Ÿ Assembly sequence facilitates OE test before
    alignment of Optical Substrate & OE components
  Ÿ Alignment procedure for human or machine vision

• Vibration Tests
  Ÿ Sine wave 10 – 2kHz at >5G (0.02 g2 / Hz), 1 hr each axis
  Ÿ No change in power supply current
  Ÿ Zero Bit Error Rate (0.0 10^-9) before & after vibration, to at least 700 Mb/s
APPLICATIONS

• Opto-electronics Applications
  Ÿ To demonstrate the feasibility of adding opto-electronic functionality and connectivity to 3D SiP
  Ÿ Initially for avionics applications
  Ÿ Incorporating an FPGA for re-programmability

• Wireless Applications
  Ÿ To demonstrate the feasibility of BlueTooth™ integration into 3D SiP
  Ÿ For automotive applications
  Ÿ Module configurable for different types of sensor & actuator
  Ÿ Data acquisition and storage
Opto-electronics Applications

e.g. Avionics, including sensors, electronic sub-systems & passenger services, for high speed / bandwidth and immunity from interference & noise (security & safety)

• Function
  Ÿ Signal processor having analogue and digital inputs & outputs
  Ÿ Bi-directional optical connection via an Opto-Electronic Level (OEL) sub-assembly on top of the 3D Stack (can not be inside a solid Cuboid)
  Ÿ Signals optical-in / electronics-out or vice versa (at either end of a link)

• Activities
  Ÿ Architecture & partitioning
  Ÿ Deployment of technology
  Ÿ Design of complex 3D Stack, including Design for Manufacture
  Ÿ Build and test
Architecture & Partitioning

• The Opto-Electronic Level (OEL) is mounted on top of the 3D Stack
  - 2 photo-receiver channels
  - 2 photo-transmitter channels
  - Optical splitter / combiner, optical I/O

• The 3D Stack has 42 active components, 32 in the 3D Stack, 10 on the OEL on top
  - Top Level : OEL, clock, comms ICs
  - Level 2 : FPGA, memory
  - Level 3 : bus ICs, etc.
  - Base Level : analogue & digital ICs

• The grouping / partitioning of the 3D Cuboid components was to:
  - Provide good electrical performance
  - Facilitate routeing of connections between related components
  - Simplify the connections on the side-walls
  - Facilitate electrical testing of individual Levels, if desirable
Deployment of Technology

• OEL Technology
  Ÿ The OEL Substrate has 4 layers:
    - Surface layer & inner signal layer, with microvias
    - Internal ground plane & backside layer for attachment to the 3D Stack
  Ÿ The OEL is attached to the 3D Stack by adhesive and soldered at perimeter holes cut across centres (as on polymer LCCs)

• Second-Level Assembly Technology
  Ÿ The base connection uses:
    - an ‘Adapter’, BGA soldered to the 3D Stack
    - a ‘Socket’, through-hole soldered to the next-level board
    - Simplifies 2nd-level assembly
    - Reduces thermal stress on 3D Stack & OEL
    - Facilitates ‘plug & play’
Design of Complex 3D Stack, including Design for Manufacture

- The 3D Stack Substrates have 10 conductor layers
  - Only BGAs need microvias, but fine features help minimise the area of the 3D Stack
  - Power & ground layer allocations finalised in line with signal routeing & thermal management
  - 174 connections between 3D Stack & motherboard, 60 power (8 voltages), 40 ground (analogue & digital)

- DfM was pursued on 3 fronts:
  - 2D Assembly – VALOR Trilogy, by SOLECTRON
  - 3D Stack Fabrication – discussion with 3D Plus
  - PCB Manufacture – discussion with PCB makers

- Thermal management by conduction:
  - Thermal vias & ground plane in each substrate
  - Down the side-wall metallisation
  - Through the Adapter / Socket to thermal vias and ground plane in the motherboard
Build and Test

• Component assembly is essentially by standard methods, except that soldering the Adapter to the finished 3D Stack uses a reflow profile optimised by SOLECTRON

• The 3D Stacks were made by 3D Plus

• The OELs were assembled by BAE Systems and tested before & after attaching to the 3D Stack

• BER measurements (optical input / electrical output & vice versa) show zero errors at 700 Mb/s, far exceeding the requirements for the application

  Ŷ Same BER results after thermal cycling, 56 x 4-hr cycles

  Ŷ Same BER results after mounted on 3D Stack & plugged into motherboard
Overview of Results

• The 3D SiP provides major reductions in area (~10X), volume (~4X) & weight (~5X) compared to a flat PCB of similar area-density.

• The OEL is 8X smaller in area than using commercially-available OE modules.

• As far as possible, the processes & sequence segments follow conventional / standard practice.

• The use of an Adapter on the base of the 3D SiP, instead of direct soldering to a motherboard:
  - Avoids exposing the heat-sensitive OE components to high temperature.
  - Reduces thermal stress on 2nd Level solder balls, the 3D Stack & the OEL.
  - Facilitates ‘plug & play’.

• We have developed a generic approach to design 3D Modules which can be applied to many kinds of future product in market sectors such as aerospace, automotive, security, industrial & high-end consumer.

• It enables integrated CAD of the 3D Stack substrates and side-walls, with full back-annotation.
Wireless Applications

• Function
  - Programmable control unit for Automotive sensor / actuator management
  - Connectivity: BlueTooth™ connectivity, 10 & 100 m ranges, CAN, RS-232, RS-485, I²C & ISO-K
  - Data acquisition & storage
  - Operation - 30 / + 85 C

• Activities
  - Architecture & partitioning
  - 2.45 GHz SMT antenna & controlled impedance lines (50 & 65 Ohms)
  - 2D & 3D designs, Design for Manufacture
  - Build and test
• Assembly Steps
  - SMT Assembly on 4 Levels
  - Assembly of BGA solder balls - 624
  - Fabrication of the 3D Module
  - Assembly of 3D Module on a motherboard

• Functional Tests
  - Circuit boards stacked in 2½D
  - Assembled 3D Module
  - Environmental exposure – Norm AEC Q100 Rev F
    - Slow Thermal cycling: -55 / +85 C, 80 hrs
    - Temp. & humidity tests (ref. A101/A110)
    - High temp. storage life (ref. JA103)
  - No functional / electrical changes
OVERALL CONCLUSIONS

• Developments in 3D SiP technology for industrialisation have been successfully introduced and demonstrated
  Ÿ Focussed on substrates, the moulding compound / encapsulant for the 3D Stack, sidewall metallisation & laser patterning.
  Ÿ Significant improvements in terms of collective process and cost savings
• Opto-electronic and wireless functionalities have been incorporated, providing additional versatility
• 3D SiP brings major reductions in area, volume & weight, with consequent cost reductions, compared to a flat PCB of similar area-density
• The 3D SiP technology can be applied to aerospace, defence, security, automotive, medical, industrial and consumer products

• We gratefully acknowledge the support of the European Commission under the Information Society Technologies (IST) part of the Fifth Framework Programme
Thank you for your attention,

do you have any questions?