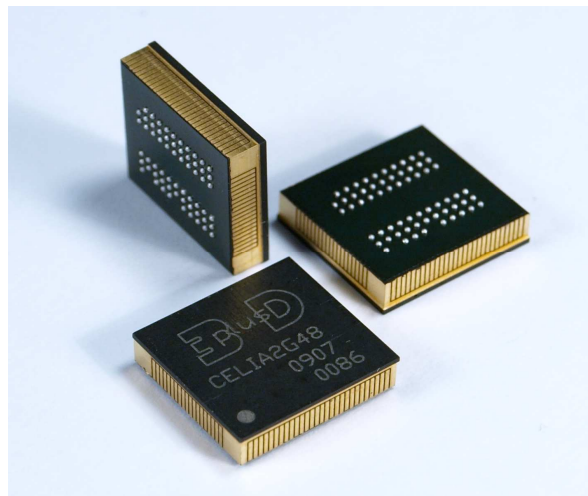


PRODUCT QUALIFICATION REPORT

3D2D2G08UB2327



Products Qualified

Products Qualified		
3D2D8G04UB2321 3D2D2G04UB2325	3D2D4G08UB2302 3D2D2G08UB2327 3D2D8G08UB2322	3D2D4G16UB2303

REVISION HISTORY			
Rev	Description of change	Author	Submit Date
1	Initial Release	Alexandre Val	01/08/2009

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1 Summary

This document describes the qualification results for the 3D2D2G08UB2327 product, a 2-stacked DDR2 memory in a 63-FBGA package.

The 3D2D2G08UB2327 product meets 3D PLUS' reliability requirements for production which is rated JEDEC MSL3 – 250°C for moisture sensitivity and Lead Free compliant.

This document serves as the qualification envelope specification for similar / derivative DDR2 stacked products.

2 Reference Documents

2.1 3D Plus Documents

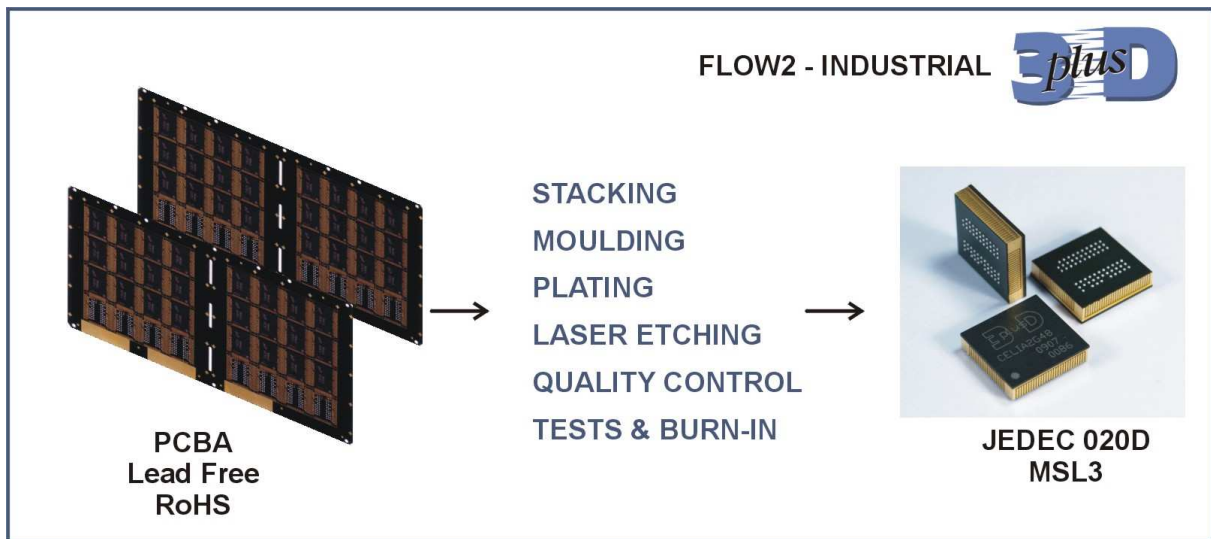
- 3300-2506-1 Evaluation Report on manufacturing of memory modules
- 3300-2663-1 Qualification Report on manufacturing of memory modules

2.2 Other Supporting Documents

- JESD22 JEDEC Standard Test Methods
- IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

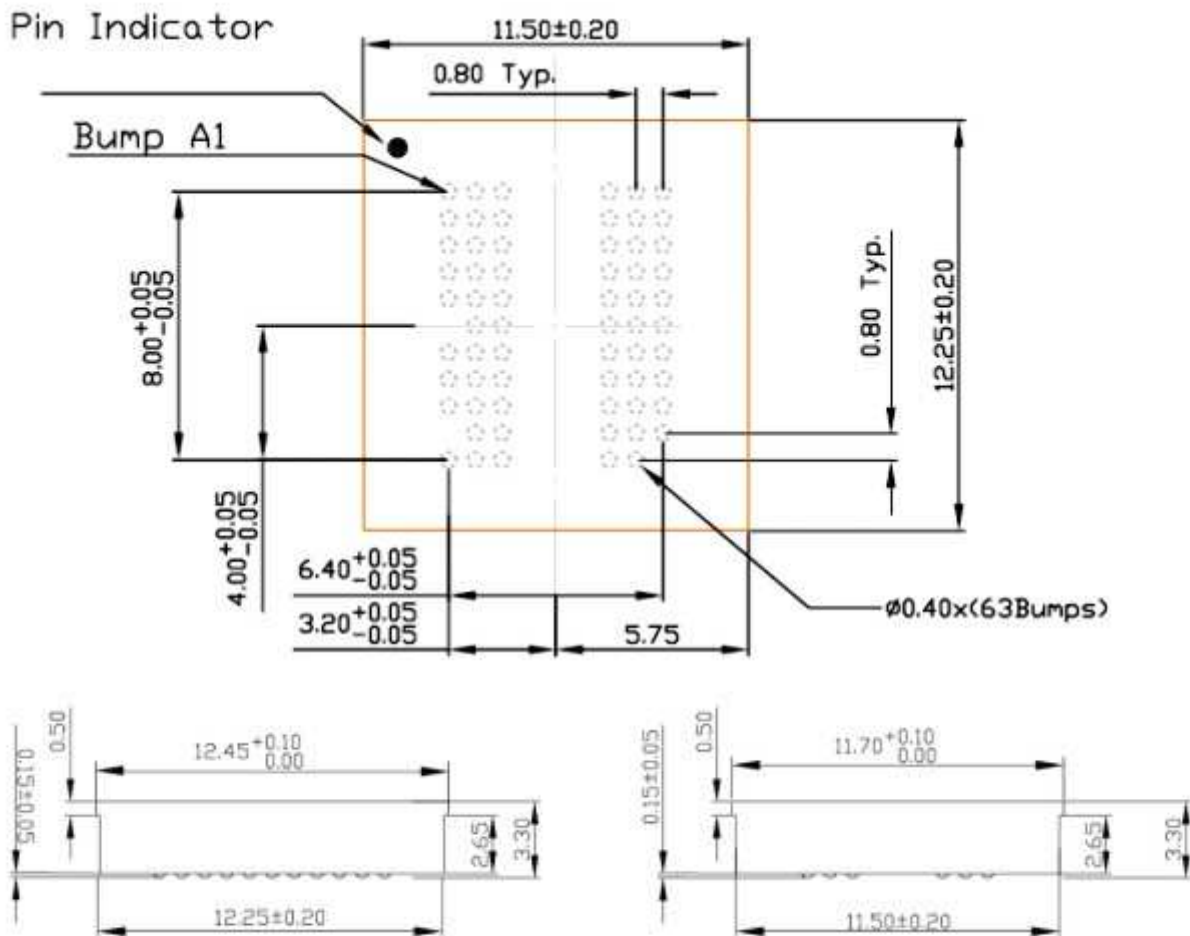
3 Fabrication Technology

These products are manufactured using 3D Plus Flow2 technology.



4 Package Definition

For product data sheet, refer to <http://www.3d-plus.com/product.php?type=4>



5 Reliability Test Procedure and Specifications

The qualification program shall consist of a minimum of two (2) independently fabricated lots. The sample size per lot is based on the concept of Lot Tolerance Percent Defective (LTPD) sampling.

For new technology, 77 pieces (3% LPTD at 90% confidence level with zero failure)

For process changes and derivatives, with the maturity of the baseline process well established, 45 pieces (3% LPTD at 75% confidence level with zero failure)

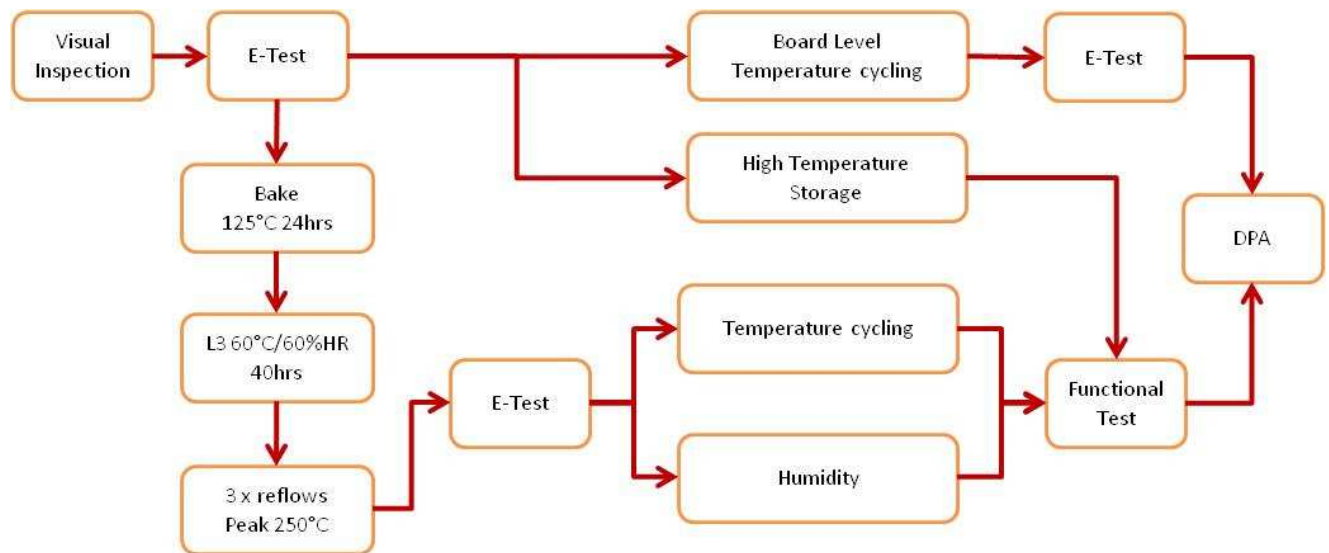
For process transfers, with respect of transferred process technology will determine 77 pieces or 45 pieces sampling plan.

In many applications, the reliability of the interaction between IC device and Printed Circuit Board (PCB) is of concern and board level testing aspects should be considered. The purpose of these board level tests is to examine the robustness of the interconnection between package and PCB.

The product, once completed assembly, is subjected to the following test procedure ; JEDEC test specifications are followed in all procedures.

Functional tests are performed at -40°C / +0°C / +2 5°C / +85°C.

Qualification flow :



6 Reliability Qualification Test Summary

6.1 High temperature storage test

Test	QTY	End Points	Results
High Temperature Storage Temp. = 125°C JESD22-A103	77 (lot 0845) 45 (lot 0905)	Continuity test at 250 500 750 1000 Functional test at 1000	Passed

6.2 Pre conditioning test

Test	QTY	End Points	Results
Pre Conditioning MSL Level3 – 250°C JESD22-A113	157 (lot 0845) 95 (lot 0905)	Bake 125°C–24hrs Moisture Soak x3 reflow Continuity test	Passed

6.3 Thermal cycles test

Test	QTY	End Points	Results
Temperature Cycling -55°C / +125°C JESD22-A104	77 (lot 0845) 45 (lot 0905) (from pre conditioning)	Continuity test at 250 500 750 1000 Functional test at 1000	Passed

6.4 Humidity test

Test	QTY	End Points	Results
Humidity 85%HR / +85°C JESD22-A101	77 (lot 0845) 45 (lot 0905) (from pre conditioning)	Continuity test at 250 500 Functional test at 500	Passed

6.5 Thermal cycles test on Board level

Test	QTY	End Points	Results
Temperature Cycling -55°C / +125°C JESD22-A104	15 x1lot 0845 32 x1lot 0905	Continuity test at 250 500 750 1500	Passed