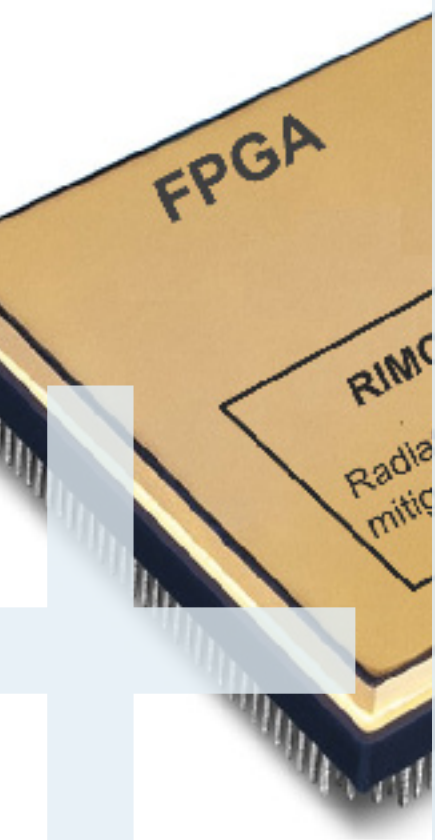
RADIATION INTELLIGENT MEMORY CONTROLLER

RIMC VHDL IP CORE
RADIATION HARDENED DDR2 SOLUTION

3DIPMC0700-1



KEY FEATURES

- High Speed (up to 400MHz) DDR2 memory controller
- Variable user data width: from x8 to x128b
- Selectable Hamming or Reed-Solomon coding schemes
- Configurable number of DDR2 ranks to increase memory capacity
- Clock & ODT settings compatible with 3D PLUS modules
- Capability to manage redundant memory designs
- Selectable Burst of 4 or Burst of 8
- DDR memory scrubbing can be enabled or disabled
- Scrubbing can be performed at a user-defined frequency
- Selectable DRAM refresh time
- Bank management algorithm instantiated inside the RIMC
- User interface AMBA® compliant (AXI/AHB/APB)
- Configurable through AMBA® interfaces
- Configurable number of AHB/AXI slave interfaces
- DDR PHY interface DFI 2.1 compliant
- Dynamically configurable via the 8-bit APB slave interface
- User can implement an AHB and/or AXI slave interface, 1 to 8 ports can be instantiated
- Provides a direct access to DDR memory array with a controller bypass mode

PRODUCT OVERVIEW

3DIPMC0700 is a fully configurable DDR2 SDRAM radiation intelligent memory controller IP core designed to work with 3D PLUS DDR2 memory modules to achieve a radiation hardened DDR2 solution. The 3DIPMC0700 can be configured to support different types of ECC for data width applications from 8b up to 128b; providing SEU mitigation and SEFI protection.

The RIMC IP Core is defined by 2 interfaces: the user interface, which is AMBA compliant, and the DDR PHY interface, compliant to DFI 2.1, to send commands and data to the DDR memory components through the DDR PHY (depends on different FPGAs). The user interface contains at least one AHB bus or AXI bus and one APB bus.

3DIPMC0700 Single Event Upset (SEU) mitigation uses different configurable ECCs (Hamming or Reed-Solomon) and scrubbing to correct SEUs and Single Event Row Errors (SERE). For example using a Reed-Solomon code for 32b data and 50% overhead [RS(12;8), m=4, Global Bus = 48bits], 3DIPMC0700 can correct up to 8 bits error (row error) in one die per 48b, and 2 SEUs in the same address of different die per 48b. In cases where scrubbing is applied, the worst case (one particle creates 2 upsets in 2 dice) error rate will be $3.8E^{-9}$ upset/day/module.

Traditionally, Single Event Functional Interruption (SEFI) mitigation has involved power cycling and/or a device reset after the occurrence of a SEFI; however, power cycling or reset will lead to data loss. To avoid data loss, a specific SEFI protection technique has been designed in the RIMC IP Core to prevent SEFI and to replace this traditional “after SEFI has happened” recovery strategy. This SEFI protection is integrated in the RIMC IP core and is transparent to the user. Verification tests have been performed to confirm the robustness of this protection IP, and no SEFI were observed up to LET>60Mev-cm²/mg.

GENERICS DESCRIPTION

NO	NAME	DESCRIPTION
1	DRAM_TYPE	Shall be set to «DDR2»
2	RTT_NOM	Nominal ODT Termination value
3	AL	Additive Latency option
4	OUTPUT_DRV	DDR3 output drive. This generic is not used for DDR2
5	HDMAX	Width of the user AMBA® busses
6	GSYNCRST	0: Asynchronous reset; 1: Synchronous reset
7	USE_DFF	0: Use block RAM inside RIMC; 1: Use DFF instead of block RAM
8	ENDIANNESS	Endianness of the AHB bus. This generic is not meaningful for AXI bus
9	SIMU	Set to 1 for simulation only
10	FREQ_RATIO	Ratio between DFIClk and SysClk. This value can be set to 1, 2 or 4
11	nCK_PER_CLK	Ratio between SysClk and DDR2 memory clock
12	BURST_LEN	Shall be 4 or 8
13	CS_WIDTH	Number od CS_N bits
14	CKE_WIDTH	Number of CKE bits
15	ODT_WIDTH	Number of ODT bits
16	CS_NUM	Number of ranks. Shall be set to 1, 2, 4 or 8 (CS_WIDTH/CS_NUM shall be an integer)
17	BANK_WIDTH	Number of banks
18	ROW_WIDTH	Number of rows
19	COL_WIDTH	Number of columns
20	NB_AHB_SLV	Number of slave AHB busses. Shall be between 0 and 8
21	NB_AXI_SLV	Number of slave AXI busses. Shall be between 0 and 8
22	DATA_WIDTH	Data width, without ECC. See Table 1 for authorized values
23	ECC_WIDTH	Width of the ECC
24	DQ_WIDTH	Width of the global DQ bus (DQ_WIDTH shall be DATA_WIDTH+ECC_WIDTH, rounded up to the next multiple of 8)

DDR2 SDRAM MODULE

DDRII P/N	DENSITY (CONFIGURATION)	VOLTAGE	PACKAGE	TEMPERATURE	SCD#
3D2D1G08US1285	1G (128M x 8b)	1.8V	SOP74	C, I, S	3DPA-6050
3D2D2G08US2662	2G (256M x 8b)	1.8V	SOP74	C, I, S	3DPA-6380
3D2D2G16UB2684	2G (128M x 16b)	1.8V	BGA95	C, I, S	3DPA-6270
3D2D4G08US4661	4G (512M x 8b)	1.8V	SOP74	C, I, S	3DPA-6090
3D2D4G72UB3652	4G (64M x 72b)	1.8V	BGA191	C, I, S	3DPA-5600
3D2D6G48UB3687	6G (128M x 48b)	1.8V	BGA143	C, I, S	3DPA-6630
3D2D6G48UQ3694	6G (128M x 48b)	1.8V	QFP144	C, I, S	3DPA-6690
3D2D8G08US8663	8G (1G x 8b)	1.8V	SOP88	C, I, S	3DPA-6100

RADIATION HARDENED DDR2 SOLUTION

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TID	-	100		krad(Si)
SEL	-	>68		MeV.cm²/mg
SEU	32b data + 16b RS ECC (GCR quiet)		$3.8E^{-9}$	error/day/module
SEFI	Under 3DIPMC0700-1 protection	>60		MeV.cm²/mg

ORDERING INFORMATION

Part Number: 3DIPMC0700 – X

Revision

3plusD a HEICO Company

www.3d-plus.com