Application Note

How to use 64Mb MRAM 3DMR64M08VS4476 in a space environment

Revision history:

Rev 1:

- initial Document

Rev2:

- I/Os protection has been added at chapter 2
- Detailed information concering SEE verification test and protection has been added at chapter 2 and 3

1. Objective

The Magneto-resistive Random Access Memory (MRAM) stores data using magnetic polarization rather than electric charge, which brings the MRAM unlimited Read/Write endurance and Single Event Upset (SEU) immune characteristics. To verify the MRAMs Single Event Effect (SEE) characteristics, several SEE campaigns have been launched by 3D PLUS at Texas A&M cyclotron. The result showed that 1Mb MRAM basic component (3D Plus Part Numbers included in the table 1) is both Single Event Latch-up (SEL) & SEU Immune.

P/N	Density	Configuration	SEE Characteristics
3DMR1M08VS1426	1M	128Kx8b	SEL LET> 80Mev.cm^2/mg; SEU Immune
3DMR2M16VS2427	2M	128Kx16b	SEL LET> 80Mev.cm^2/mg; SEU Immune
3DMR4M08VS4428	4M	512Kx8b	SEL LET> 80Mev.cm^2/mg; SEU Immune
3DMR8M32VS8471	8M	256x32b	SEL LET> 80Mev.cm^2/mg; SEU Immune
3DMR8M32VS8420	8M	256x32b	SEL LET> 80Mev.cm^2/mg; SEU Immune

Table 1: SEL & SEU Immune MRAM

Meanwhile, High Current Event has been observed at the test of 16Mbit elementary component of the module 3DMR64M08VS4476 (More information can be found at: http://www.3d-plus.com/doc/prod/3dfp_0476_2.pdf). The test result also confirmed that this MRAM memory cell is SEU immune > 85Mev.cm2/mg. Hereby is the LET threshold and Saturated Cross Section of this High Current Event:

High Current Event LET Threshold > 8.3Mev.cm2/mg at 3.6V V_{DD} and +85°C;

Saturated Cross Section: 1E-03cm2/Device

The calculation has been done to show the event rates [(1)] at different orbits:

Adams 90 GEO orbit event rate: 1.5 event/year

LEO Pol orbit (98°, 800km, 800km) event rate: 1.6 event/year

MEO orbit (63.4°, 1000km, 26768km) event rate: 0.6 event/year

Note1: The error rates have been calculated at worst case: assuming the MRAM is permanently powered.

Therefore, 3D PLUS recommends using this 3DMR64M08VS4476 in conjunction with a High current limiter function.

2. Use of 3DMR64M08VS4476 with 3D PLUS Latch-up Current Limiter Module

The 3D PLUS Latch-up Current Limiter (LCL) 3DPM0168 monitors the power supply line of the device and switches it off instantaneously to protect the device in case of any overvoltage or overcurrent occured. The LCL provides 2 adjustable current thresholds (Run & Standby) by external resistors and Manual or Automatic reconnection (after a delay adjustable by the user through external capacitor). More information can be found at: http://www.3d-plus.com/product.php?type=7

To protect the 3DMR64M08VS4476 from High Current Event, 2 configuration2 have been considered. Block diagram is shown in figure 1.

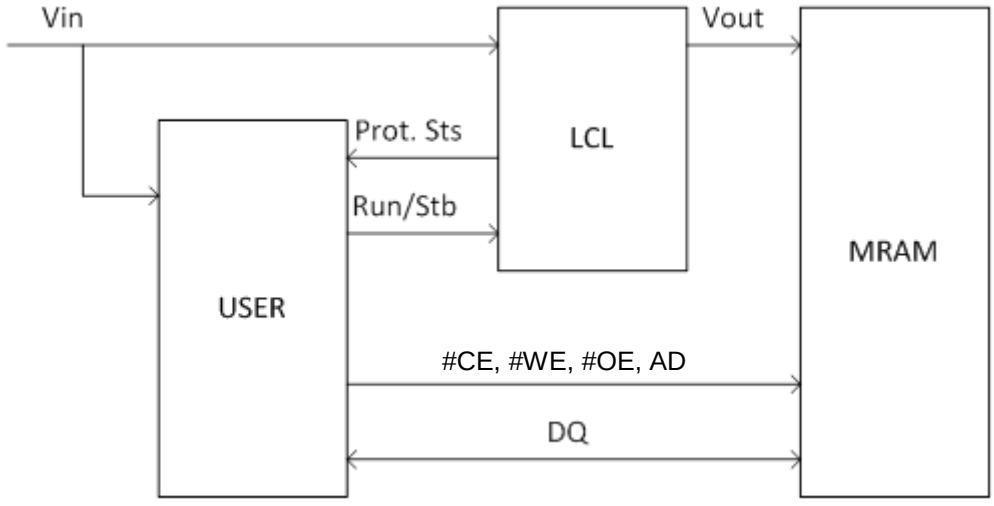

Figure1: LCL protected MRAM Block Diagram

Configuration 1: 3DMR64M08VS4476 used as data buffer in Read/Write mode

In this case, two thresholds (100mA & 200mA) and an automatic reconnection with a 300ms delay are recommended. LCL configuration is shown below:

LCL Pin	Description	Configuration
ADJ_RESTART	Input pin used to select the automatic restart function provided by the LCL and to adjust the delay. When connected directly to GND, automatic restart function is inhibited. When connected to a capacitor, automatic restart is selected. Capacitor value set the delay for automatic reconnection.	Connect to a 6µF Capacitor to set a 300ms delay
RUN/STB	Input pin used to select the active current protection threshold. When this pin is connected to a low level voltage, low level current threshold corresponding to standby mode is selected (Ith_stb). When this pin is connected to a high level voltage, high level current threshold corresponding to run mode is selected (Ith_run).	Input low voltage to select the low current threshold 100mA; Input high voltage to select the high level current threshold 200mA;
LIM_RUN	Pin used to set the high level current threshold (Ith_run). Ith_run value is set by a resistor connected between this pin and the LIM_STB pin.	30kΩ resistor between LIM_RUN and the LIM_STB pin
LIM_STB	Input pin used to set the low level current threshold (Ith_stb). Ith_stb value is set by a resistor connected between this pin and GND.	40kΩ resistor between LIM_STB and GND
PROT_STATUS	Output Protection Status pin. This signal at this pin is used to monitor the LCL state. Signal is pulled to GND when LCL is not tripped. Signal is pulled to high level when LCL is tripped (load disconnected after overcurrent).	-

Configuration 2: 3DMR64M08VS4476 used as a read-only memory:

In this case, only one protection threshold (100mA) and an automatic reconnection with a 300ms delay are recommended. LCL configuration is shown below:

LCL Pin	Configuration
ADJ_RESTART	Connect to a 6µF Capacitor to set a 300ms delay
RUN/STB	Input Low Voltage
LIM_RUN	Open
LIM_STB	40kΩ resistor between LIM_STB and GND
PROT_STATUS	-

An example configuration 2 is 3DMR64M08VS4476 used as the configuration memory of a Xilinx Virtex FPGA and protected with one LCL 3DPM0168.

In any case, the protection on all MRAM I/Os is recommended, which means cutting I/Os (ex: active the high-impedance of the FPGA tri-state buffers which connect to MRAM I/Os) based on LCL PROT_STATUS to prevent the current flow through the I/Os when radiation High Current Event happened.

3. SEE verification test

Additional SEE verification test has been performed at Texas A&M cyclotron. Block diagram as shown in figure 1 was implemented with 3DMR64M08VS4476 basic component: 16Mb MRAM die and LCL 3DPM0168. The results were: with the LCL, the 16Mb MRAM die is protected for fifty events with a let

of 85.4Mev.cm2/mg. Moreover, No SEU observed with the LET value of 85.4Mev.cm2/mg when the device is in power down mode or in standby mode.

4. Conclusion

The 64Mb MRAM 3DMR64M08VS4476 is naturally SEU immune. High Current Events can occur with a rate of 1.5 event/year in Adams 90 GEO orbit.
3D Plus recommends to protect the 64Mb MRAM 3DMR64M08VS4476, including power supply and all I/Os, with LCL module 3DPM0168.

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