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**MEMORY MODULE**

**EEPROM**

3DEE5M40VS5257

5 Mbit: 40-bit bus width, EEPROM based on 128K x 8

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**GENERAL DESCRIPTION**

The 3DEE4M40VS5257 is a 5 Mbit EEPROM (Electrically Erasable and Programmable ROM) organized as a single bank of 128K x 40 bits. This bank 40-bit interface is selected with #CE0. All other signals are common to the five 1 Mbit EEPROM memories.

Using high performance and high reliability CMOS technology combined with 3D PLUS patented stacking technology, this EEPROM memory is well suited for use in high reliability, high performance system applications.

The module packaged in a SOP 64 is available for Commercial, Industrial or Military temperature range. It is also available with screening options up to space grade level.

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**KEY FEATURES**

Memory Cell Array 128K x 40 bits

- 3.3 V single power supply
- Access time: 250 ns (Max)
- Power dissipation
  - Active: 100 mW/Hz (Typ)
  - Standby: < 0.5 mW (Max)
- On-chip latches: address, data, #CE, #OE, #WE
- Single voltage operation: 3.3 V
- Automatic byte write: 15 ms (Max)
- Automatic page write (128 bytes): 15 ms (Max)
- Command/Address/Data Multiplexed I/O Port
- Data polling and RDY/#BUSY
- Endurance: 100k Program/Erase Cycles
- Data Retention: 10 Years
- Software data protection
- Write protection by #RES pin
- Available temperature range
  - 0°C to +70°C
  - -40°C to +85°C
  - -55°C to +125°C
- Available with screening options up to grade S
- ITAR free

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**PIN ASSIGNMENT** (top view)

**FUNCTIONAL BLOCK DIAGRAM**

![Functional Block Diagram](image)

All other signals are common to the five memories.
MEMORY MODULE

EEPROM

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MECHANICAL DRAWING

DC Operating Conditions and Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>2.70</td>
<td>5.50</td>
<td>V</td>
</tr>
<tr>
<td>Input logic High Voltage</td>
<td>$V_{IH}$</td>
<td>1.90</td>
<td>$V_{CC} + 0.30$</td>
<td>V</td>
</tr>
<tr>
<td>Input logic Low Voltage</td>
<td>$V_{IL}$</td>
<td>-0.30</td>
<td>0.80</td>
<td>V</td>
</tr>
<tr>
<td>Output logic High Voltage</td>
<td>$V_{OH}$</td>
<td>0.80 x $V_{CC}$</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Output logic Low Voltage</td>
<td>$V_{OL}$</td>
<td>—</td>
<td>0.40</td>
<td>V</td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage relative to $V_{SS}$</td>
<td>$V_{IN}$</td>
<td>-0.5 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{STG}$</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_J$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal resistance, junction to case</td>
<td>$R_{TH(J-C)}$</td>
<td>10</td>
<td>°C/W</td>
</tr>
<tr>
<td>Power dissipation permitted (1)</td>
<td>$P_D$</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>

(1): $P_D = (T_{JC(max)} - T_{C(max)}) / R_{TH(J-C)}$ as per definition of MIL-STD-883, Method 1012

DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>One bank operating current @ 1 MHz</td>
<td>$I_{CC3_{1MHz}}$</td>
<td>75 mA</td>
<td></td>
</tr>
<tr>
<td>TTL standby current</td>
<td>$I_{CC2}$</td>
<td>5 mA</td>
<td></td>
</tr>
<tr>
<td>CMOS standby current</td>
<td>$I_{CC1}$</td>
<td>100 μA</td>
<td></td>
</tr>
</tbody>
</table>

3DEE5M40VS5257

Temperature Range

C = (0°C to +70°C)
I = (-40°C to +85°C)
M = (-55°C to +125°C)
S = Specific

Quality Level

N = Commercial Grade
B = Industrial Grade
S = Space Grade

MODULE MARKING

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DISTRIBUTOR

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